ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 7, Issue 1, January 2018

A Comparative Analysis of Different Approximate Adders Used for Image Compression and Image Addition

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Abstract—**With the increase in the number of components on the circuit, it can no longer sustain Moore's law that further lead to huge power dissipation. One of the major areas where the power dissipation is large is image compression. So for the applications where exactness is not required, approximate implementation of circuit is considered as the solution. To reduce the power dissipation, exact adders are replaced by the approximate adders for the low power imprecise applications. In this review paper, a comparative analysis of various approximate adders is carried out based on the parameters such as error distance, transistor count, number of erroneous outputs and many more.**

Index Terms—**Approximate adders, low power, erroneous outputs, error distance, transistor count.**

I. INTRODUCTION

In today's era, in applications where exactness at outputs are not required are increased so the researchers are more interested to work on this field. The major backbone of all the multimedia devices are Digital Signal Processing (DSP) blocks and most of the DSP blocks are implementing image processing algorithms. Algorithmic noise tolerance (ANT) [1] [2] [3] [4], significance driven computation (SDC) [5] [6] [7] and non-uniform voltage over- scaling (VOS) [8] are the various low power design through approximate computing at the algorithm and architecture level [9]. Therefore, to reduce the power dissipation at the circuit level, various adders are approximated and an inexact adder cells are used to replace the exact adders. Image compression is the most common technique in the multimedia and the major block of the image compression is Discrete Cosine Transform (DCT) which comprises of adders and multipliers that are very power consuming.

Manuscript received Jan , 2018.

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That is why approximate adders are used in the image compression because human in image compression human beings can collect useful information from slightly erroneous outputs. First is the complexity reduction of the Mirror Adder which is mostly used implementation of full adder, is approximated at the transistor level. The main advantage of the approximations of the Mirror Adder is that it reduced the number of transistors in the circuit but also reduced the internal node capacitances which led to shorter delay [9]. Secondly, to replace the exact adders, XOR/XNOR based adders are used. In XOR/XNOR based approximate adders the approximation is done on the 10-transistor based accurate full adder [10]. Third is to replace the full adder cell with the inexact adder cells which have less number of transistors than the exact adder cell design [11]. So to compare various approximate adders parameters like transistor count, number of erroneous outputs and error distance are taking into account.

II. JPEG IMAGE COMPRESSION AND DECOMPRESSION

Joint Photographic Experts Group (JPEG) is the commonly used method of compression for the digital images, particularly for the images produced by digital photography [12].

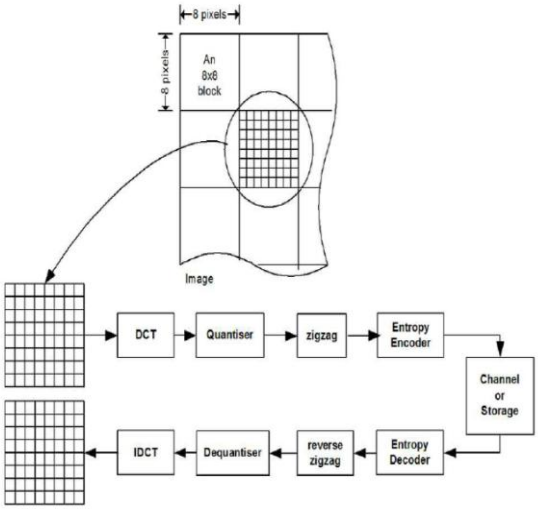

Fig. 1 JPEG compression and decompression

It is seen that that Discrete Cosine Transform (DCT) is basic step in the image compression. DCT block only consist adders

and multipliers. In the image compression the image is converted into the frequency domain by the DCT which separate images into parts of different frequencies. The DCT is one to one mapping between image and frequency domain [12]. The working of the quantized is that it converted the DCT matrix into the identity matrix and after that, it is encoded and pass to channel or storage.

III. APPROXIMATE ADDERS

The adders play a key role in determining the speed and power consumption of Digital Signal Processing (DSP) systems. The demands of high speed and power efficiency as well as the fault tolerance nature of some applications such as image compression have promoted the development of approximate adders.

A. The Mirror Adder

As the Mirror Adder is the widely economical representation of the Full Adder (FA) [13], so it is the basis for all different approximations of the FA cell [9].

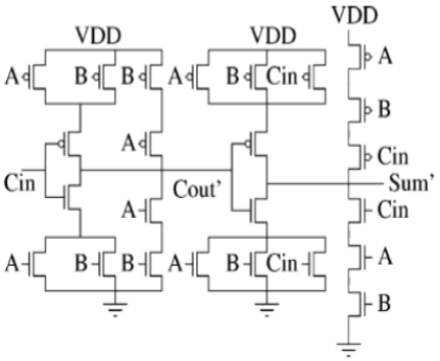

Fig. 2 Conventional Mirror Adder [9]

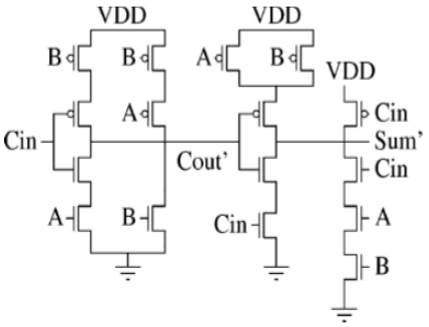

Fig. 3 MA Approximation 1 [9]

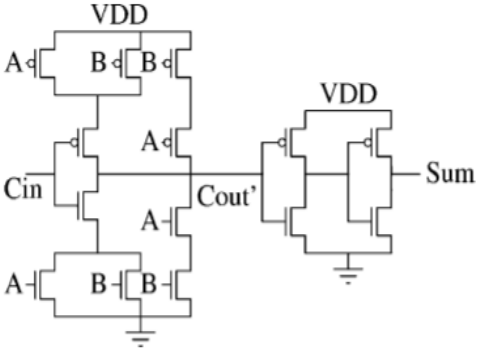

Fig. 4 Mirror adder approximation 2 [9]

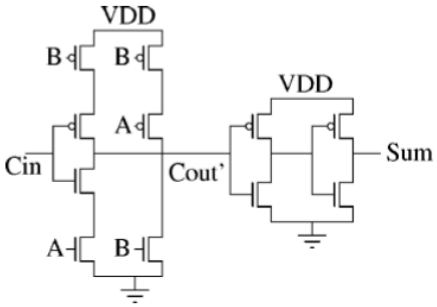

Fig. 5 Mirror adder approximation 3 [9]

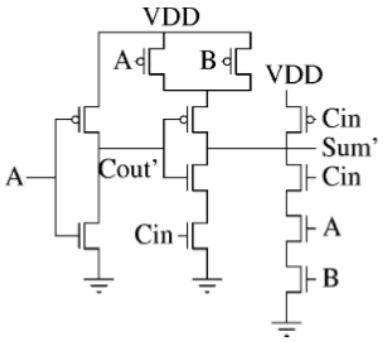

Fig. 6 Mirror adder approximation 4 [9]

It is seen in the mirror adder structure that the series connected transistors contribute to larger delay. Therefore, removal of some of them will facilitate faster charging/discharging of node capacitances. By removing some of series connected transistors, it led to reduction of the switched capacitance in the dynamic power expression. There are total number of 24 transistors in the conventional mirror adder.

1 Approximation 1

For the approximation 1, transistors is removed one by one from conventional Mirror Adder but it is to ensure that the input combination of A, B and Cin does not get short circuit or open circuit in the simplified mirror adder. It should be take care of that there should be minimal errors in the FA truth table [9]. Therefore by applying the above steps there should be 8 less transistors as compared to the conventional Mirror Adder as shown in Fig.2.

2 Approximation 2

Except for A=0,B=0,Cin=0 and A=1,B=1,Cin=1, Sum=Cout1 from the truth table 1 [9]. In the conventional Mirror Adder, Cout bar is computed [9]. Thus for the simpler schematic take Sum= Cout bar. The reason for the buffer stage after Cout in the conventional MA is that the total capacitances at the sum node would be a combination of four source-drain diffusion and two gate capacitances which lead to delay penalty in case where two or more multi-bit adders are connected in series [9].

3 Approximation 3

Approximation 3 is obtained by combining approximations 1 and 2 as shown in Fig.4.

4 Approximation 4

From six out of eight cases in the FA truth table, Cout=A and for another six cases Cout=B [9]. So A and B are

Table 1 Truth table for the conventional MA and its Approximations 1-4 [9]

Inputs			Accurate outputs		Appropriate outputs					
A	B	Cin	Sum	Cout	Sum1	Cout1	Sum2	Cout2	Sum3	Cout3
0	0	0	0	0	1(F)	0	0	0	0	0
0	0	1	1	0	1	0	1	0	0(F)	0
0	1	0	1	0	0(F)	1(F)	0(F)	0	1	0
0	1	1	0	1	0	1	1(F)	0(F)	1(F)	0(F)
1	0	0	1	0	1	0	0(F)	1(F)	0(F)	1(F)
1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	1(F)	1
1	1	1	1	1	0(F)	1	1	1	1	1

interchangeable, therefore take Cout=A [9]. To calculate the Cout bar, use inverter at input A and sum is calculated as the approximation 1.

From the above truth table it can clearly see that in the approximation 1, there are 3 errors in sum1 and 1 one error in Cout as compared to conventional MA. In the approximation 2, there are 3 errors in the sum 2 and 2 errors in Cout as compared to the conventional MA. In the approximation 3, there are 4 errors in the sum and 2 errors in the Cout as compared to conventional MA. Approximation 3 is having lesser area as compared to the others and have better node capacitances.

B. XOR/XNOR based adders

The approximate XOR/XNOR based on 10-transistor full adder [14]. It has total number of 10 transistors with X, Y and Cin as inputs and I as an internal signal.

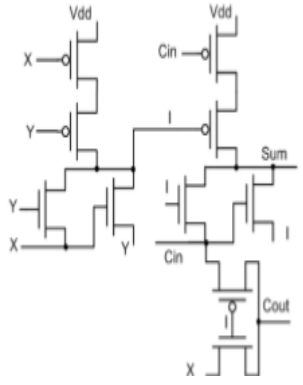

Fig.7 Accurate full adder with 10 transistors [14]

1. Approximate XOR based adder 1(AXA1)

In the AXA1, XOR operation is performed by an inverter and two pass transistors that are connected to X and Y respectively [10]. When Y is "1", I is equal to X bar otherwise I is equal to X bar that is I is equal to X XOR Y [10]. The total error distance in the AXA1 is 4.

$$Sum = C_{in},$$
$$C_{out} = \overline{(X \oplus Y)C_{in} + \bar{X}\bar{Y}}.$$

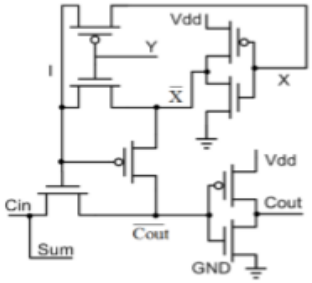

Fig.8 Approximate XOR-based adder 1(AXA1) [10]

2. Approximate XNOR based adder 2 (AXA2)

AXA2 is the approximate adder with 6 transistors and it consists of 4-transistor XNOR gate and a pass transistor [10]. AXA2 has the error distance of 4. In the Sum and the Cout signals there are some transitions, which do not have full swing due to threshold voltage drop in some of the pass transistors [10].

$$Sum = \overline{(X \oplus Y)}C_{in},$$
$$C_{out} = (X \oplus Y)C_{in} + XY$$

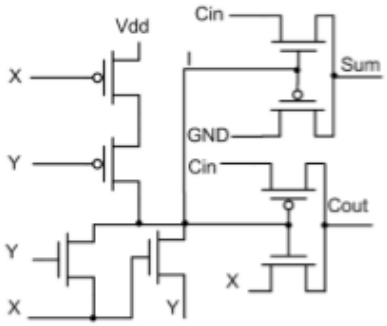

Fig.9 Approximate XNOR-based adder 3(AXA3) [10]

3. Approximate XNOR based adder 3 (AXA3)

AXA3 is the extension of the AXA2, which are having 2 more transistors in pass transistors for better accuracy of sum [10]. From all of 8 transistors, 4 are utilized in the XNOR gate. AXA3 has the error distance of 2, which is minimum among all the approximations.

$$Sum = \overline{(X \oplus Y)}C_{in},$$
$$C_{out} = (X \oplus Y)C_{in} + XY$$

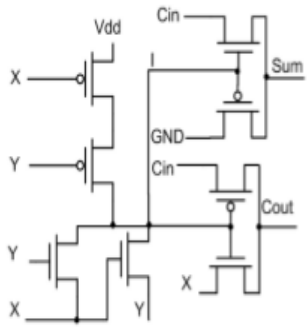

Fig.10 Approximate XNOR-based adder 3(AXA3) [10]

Table 2 Truth table and the error distance of AXAs [10]

X	Y	Cin	Accurate adder		AXA1			AXA2			AXA3		
			Cout	Sum	Cout	Sum	ED	Cout	Sum	ED	Cout	Sum	ED
0	0	0	0	0	0	0	0	0	1	1	0	0	0
0	0	1	0	1	0	1	0	0	1	0	0	1	0
0	1	0	0	1	1	0	1	0	0	1	0	0	1
0	1	1	1	0	0	1	1	1	0	0	1	0	0
1	0	0	0	1	1	0	1	0	0	1	0	0	1
1	0	1	1	0	0	1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0	1	1	1	1	0	0
1	1	1	1	1	1	1	0	1	1	0	1	1	0

C. Inexact adder cells

As compared to the exact adder cells, inexact adder cells require less number of transistors [9] [10]. There are three inexact adder cells named InXA1, InXA2 and InXA3 [11].

1. First Inexact adder cell (InXA1)

In the InXA1 only carry is approximating and sum is retained as the exact sum [11].

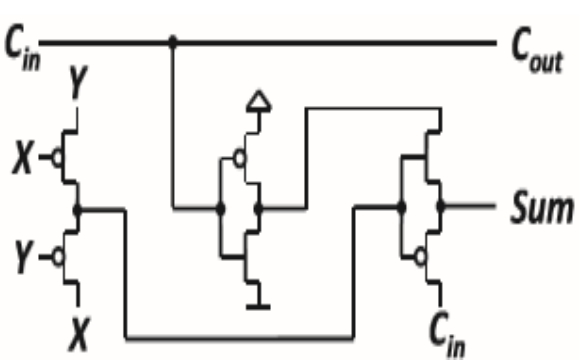

Fig.11 Transistor circuit diagram of InXA1

2. Second Inexact adder cell (InXA2)

In InXA2, sum is approximated and the carry is exact.

3. Third Inexact adder cell (InXA3)

In the InXA3 there is the approximation into the sum while the carry is exact. When compared to the exact full adder cell, InXA2 reduces the gate delay [11].

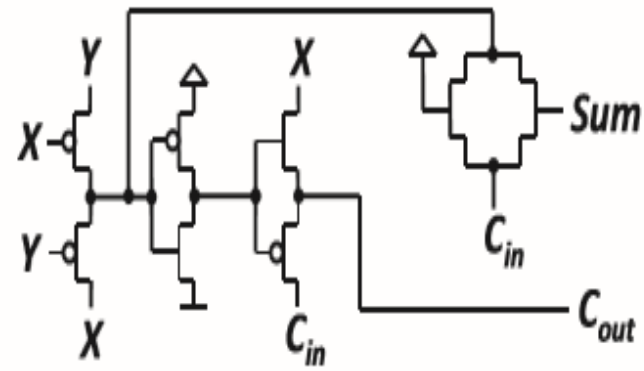

Fig.12 Transistor circuit diagram of InXA2

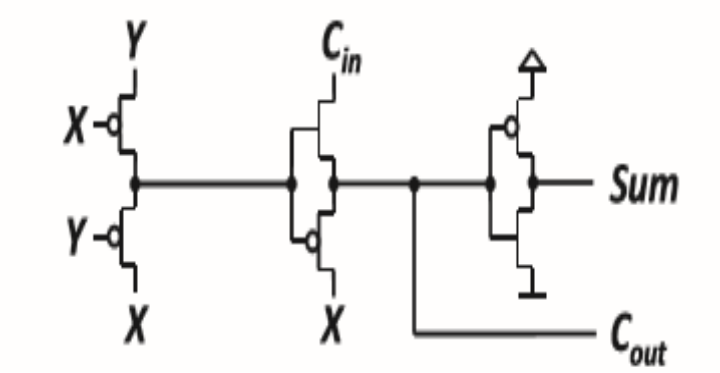

Fig.13 Transistor circuit diagram of InXA3

Table 3 Truth table of the inexact adder cells compared with exact adder cell

Inputs			Exact Outputs		Proposed Inexact Adder Cells					
					InXA1		InAX2		InAX3	
X	Y	Cin	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout
0	0	0	0	0	0	0	0	0	1(F)	0
0	0	1	1	0	1	1(F)	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	1(F)	1	0	1
1	0	0	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1(F)	1	0	1
1	1	0	0	1	0	0(F)	0	1	0	1
1	1	1	1	1	1	1	1	1	0(F)	1

As from the truth table it is seen that the InXA1 introduce errors in rows 2 and 7 while InXA2 introduces error in sum at rows 4 and 6. In case of InXa3, errors are only introduced at rows 1 and 8 as compared to the exact adder cell.

Table 4 Comparison of all the approximate adders [9] [10] [11]

Metric		AMA1 [1]	AMA2 [2]	AMA3 [2]	AMA4 [2]	AXA1 [3]	AXA2 [3]	AXA3 [3]	InXA1 [4]	InXA2 [4]	InXA3 [4]
Number of transistors		20	14	11	15	-	-	-	6	8	6
Transistor Count		16	14	11	-	8	6	8	-	-	-
Number of erroneous values	sum	2	2	3	3	-	-	-	0	2	2
	Carry	1	0	1	2	-	-	-	2	0	0
Delay for sum		-	-	-	-	0	20.16	61.82	-	-	-
Total error distance		3	3	4	-	4	4	2	-	-	-

CONCLUSION

As the image processing is the most common technique in the multimedia. The major block of the image compression is Discrete Cosine Transform (DCT) which comprises of adders and multipliers that are very power consuming. That is why approximate adders are used instead of the accurate adders in the DCT. The approximate adders discussed are the Mirror adder; XOR/XNOR based adders and the inexact Adder cells. From all of the approximate adders, the inexact adder cells gives better results in terms of less number of transistors, transistor count and number of erroneous outputs. So by using the approximate adders, power consumption and delay can be reduced to certain amount in the human sensitive applications.

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