ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 7, Issue 2, January 2018

Study & Comparison Analysis of SRAM at 65nm and 90nm Technology

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Abstract: In this paper we are analyzing the simulation of the 6T SRAM Cell in 65nm & 90nm Technology using TANNER EDA tool and Micro wind. We are using simulations results of variations in power and Delay with two cases,
(i) Variation in VDD
(ii) Variation on Temperature.

***Keywords*—VLSI, Micro Wind, Tanner EDA, VDD, SRAM, Delay, Power, Temperature**

I. INTRODUCTION

The process of placing hundreds of thousands of electronic components on a single chip is used to define VLSI. Almost all modern chips employ VLSI architectures, or ULSI (ultra large scale integration). An SRAM (Static Random Access Memory) is designed to fulfill two basic needs (a) to provide a direct interface with the CPU at speeds not attained by DRAMs and (b) to replace RAMs in systems that require very low power consumption [3]. In the first case, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. Figure 1 shows a typical PC microprocessor memory configuration.

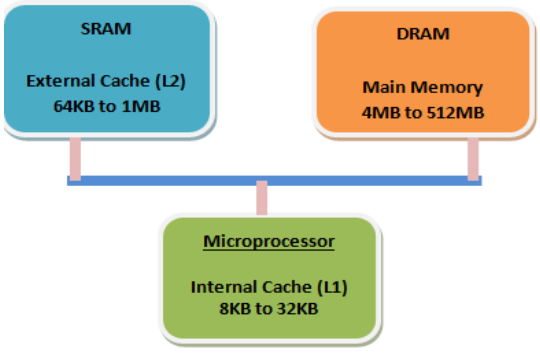

Figure 1 Typical PC microprocessor memory Configuration

Typical Fast low power SRAMs have become a critical component of many VLSI chips now-a-days. This is valid for microprocessors, where the on-chip cache sizes are growing with each generation so as to bridge the increasing divergence in the speeds of the processor and the main memory. Simultaneously, power dissipation has also become an important consideration both due to the increased integration and operating speeds [5].

Manuscript received Jan , 2018.
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DESIGN OF 6T SRAM Cell

Cell Structure

The conventional six-transistor (6T) SRAM is built up of two cross coupled inverters and two access transistors, connecting the cell to the bit lines as shown (Figure 2). The inverters make up the storage element and the access transistors are used to communicate with the outside circuitry. No special process steps are needed and it is fully compatible with standard CMOS processes [6].

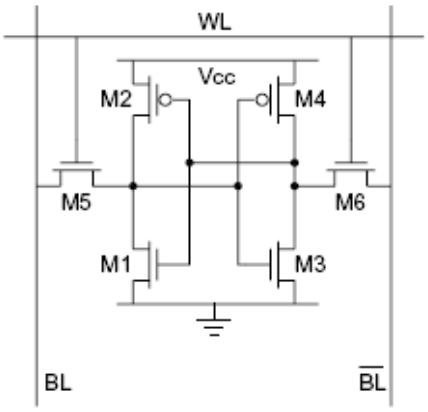

Figure 2 6T SRAM cell

Read Operation

The 6T SRAM cell utilizes a differential read operation. This means that both the stored value and its inverse are used in evaluation to determine the stored value.

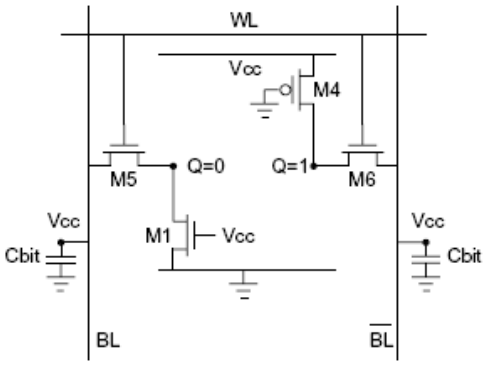

Figure 2 6T SRAM cell

Before the onset of a read operation, the word line is held low (grounded) and the two bit lines connected to the cell through transistors M5 and M6 (see Figure 3) are pre-charged high (to VCC). As the gates of M5 and M6 are held low, these

access transistors are off and the cross-coupled latch is isolated from the bit lines.

If a ’0’ is stored on the left storage node, the gates of the latch to the right are made low. That means that transistor M3 (see Figure 3) is initially turned off. In the same way, M2 will also be off initially since its gate is held high [5]. This results in a simplified model, shown in Figure 3, for reading a stored ’0’. In the Figure 3 the capacitors C-bit represents the capacitances on the bit lines, which are several magnitudes larger than the capacitances of the cell. The cell capacitance has here been represented only through the value held by each inverter (Q=0 and Q=1 respectively). The next phase of the read operation scheme is to pull the word line high and at the same time release the bit lines. This turns on the access transistors (M5 and M6) and connects the storage nodes to the bit lines. It is evident that the right storage node (the inverse node) has the same potential as /BL and therefore no charge transfer will be take place on this side. The left storage node, on the other hand, is charged to ’0’ (low) while BL is pre-charged to VCC. Since transistor M5 now has been turned on, a current is going from C-bit to the storage node. This current discharges BL while charging the left storage node. As mentioned earlier, the capacitance of BL (C-bit) is far greater than that of the storage node. This means that the charge sharing alone would lead to a rapid charging of the storage node, potentially destroying the stored value, while the bit line would remain virtually unchanged. However, M1 is also turned on which leads to a discharge current from the storage node down to ground. By making M1 stronger (wider) than M5, the current flowing from the storage node will be large enough to prevent the node from being charged high. After some time of discharging the bit line, a specialized detection circuit called Sense Amplifier
(see Figure 3) is turned on [2].

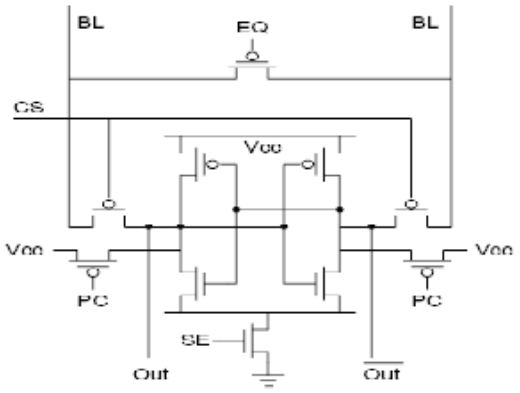

Figure 4: Sense Amplifier for a six-transistor SRAM.

It detects the difference between the potentials of BL and /BL and gives the resulting output. Initially the sense amplifier is turned off (sense enable, SE, is low). At the same time as the bit lines of the 6T cell are being pre-charged high, so are the cross-coupled inverters of the sense amplifier. The bit lines are also equalized (EQ is low) so that any mismatch between the pre-charges of BL and /BL is evened out. When the word line of the memory cell is asserted EQ and PC are lifted and the pre-charge of the sense amplifier is discontinued. The column selector CS is then lowered to connect the bit lines to the latch of the sense amplifier. In Figure 4, for purpose of clarity, only one column selector transistor for each side of the sense amplifier is present. However, normally several bit lines are connected to the same sense amplifier, each one with its own column selector transistor. In this way, several bit lines can be connected to the same sense amplifier, and the column selectors are then used to determine which bit lines should be read. After some time, when a voltage difference of about 50-100mV (for a 0.18um process) has developed between the two inverters of the sense amplifier, the sensing is turned on. This is done by raising SE, and thereby connecting the sources of the NMOS transistors in the latch to gnd. Since the internal nodes were pre-charged high the NMOS transistors are open and current is being drawn from the nodes. The side with the highest initial voltage will make the opposite NMOS (since it is connected to its gate) draw current faster. This will make the lower node fall faster and in turn shut of the NMOS drawing current from the higher node. An increased voltage difference will develop and eventually the nodes will flip to a stable state [4].

The Out node in Figure 4 is then connected to a buffer to restore the flank of the signal and to facilitate driving of larger loads. Also the out node is usually connected to an inverter. This inverter is of the same size as the first inverter in the buffer. This is to make sure that the two sense amplifier nodes have the same load, and therefore will be totally symmetric. Note that it is essentially the ’0’ that is detected for the standard 6T SRAM, since the side with the stored ’1’ is left unchanged by the cell. The output is determined by which side the ’0’ is on; ’0’ on the normal storage node results in a ’0’ output while ’0’ on the inverse storage node results in a ’1’ output. Therefore the performance is mainly dependent on the constellation M1-M5 (see figure 3.1) or M3-M6 and their ability to draw current from the bit line. Suppose I_1 and I_5 are the currents flowing in the cell and V_q be the node voltage, then we can calculate the voltage stored at the node by equating these two equations as follows [1]:

$$I = \mu_n . c_{ox} (W/L)_1 [(V_{DD} - V_{t1}) v_q - 1/2\ v_q^2] \ldots\ldots\ldots\ldots (1)$$

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 7, Issue 2, January 2018

$$I_5 = 1/2\mu_n.c_{ox}\,(W/L)_5(V_{DD} - v_q - V_{t5})^2 \ldots\ldots\ldots\ldots (2)$$

V_q is the desired voltage through we can estimate that the value of current I_1 or I_5. Power dissipation can be calculated by multiplying current I_5 with voltage supplied equal to 1.8V. Similar is the case in write operation.

Write Operation

For a standard 6T SRAM cell, writing is done by lowering one of the bit lines to ground while asserting the word line. To write a '0' BL is lowered, while writing a '1' requires BL to be lowered. Why is this? Let's take a closer look at the cell when writing a '1' (Figure 5). As in the previous example of a read, the cell has a '0' stored and for simplicity the schematic has been reduced in the same way as before. The main difference now is that the bit lines no longer are released. Instead they are held at VCC and GND respectively. If we look at the left side of the memory cell (M1-M5) it is virtually identical to the read operation (Figure 3). Since both bit lines are now held at their respective value, the bit line capacitances have been omitted. During the discussion of read operation, it was concluded that transistor M1 had to be stronger than transistor M5 to prevent accidental writing [7].

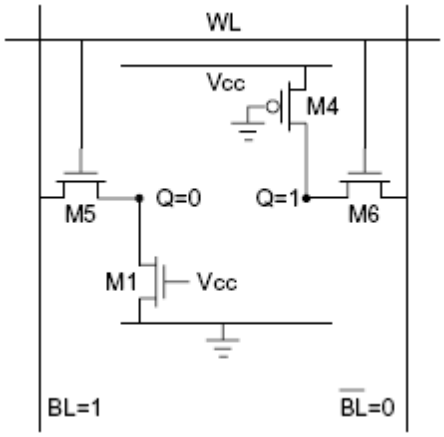

Figure 5 Six-T SRAM cell write operation (Writing '0' to '1').

In the write state, this feature actually prevents a wanted write operation. Even when transistor M5 is turned on and current is flowing from BL to the storage node, the state of the node will not change. As soon as the node is raised transistor M1 will sink current to ground, and the node is prevented from reaching even close to the switching point. So instead of writing a '1' to the node, we are forced to write a '0' to the inverse node. Looking at the right side of the cell we have the constellation M4 M6. In this case /BL is held at gnd. When the word line is raised M6 is turned on and current is drawn from the inverse storage node to /BL**.** At the same time, however, M4 is turned on and, as soon as the potential at the inverse storage node starts to decrease, current will flow from VCC to the node. In this case M6 has to be stronger than M4 for the inverse node to change its state. The transistor M4 is a PMOS transistor and inherently weaker than that of the NMOS transistor M6 (the mobility is lower in PMOS than in NMOS). Therefore, making both of them minimum size, according to the process design rules, will assure that M6 is stronger and that writing is possible. When the inverse node has been pulled low enough, the transistor M1 will no longer be open and the normal storage node will also flip, leaving the cell in a new stable state [9].

II. CIRCUIT DIAGRAM

Figure 6 shows schematic of a typical 6T SRAM Cell. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional *access* transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit. Access to the cell is enabled by the word line (WL in Figure 6) which controls the two access transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and /BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins [8].

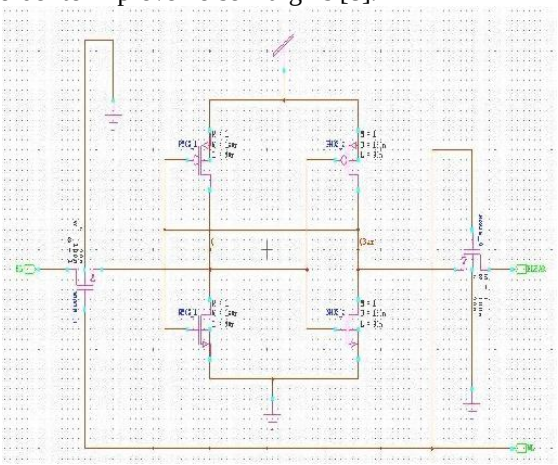

Figure 6 Schematic of 6T SRAM Cell

In this Schematic of 6T SRAM which is drawn in the S-EDIT in Which 2 PMOS and 4 NMOS Transistors are used. The Length & Width are

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define like Length is equal to the technology and width is approximately double to the length. Here are three inputs in this circuit WL, BL, /BL and two outputs are obtained Q and QBAR. In this WL is equal to VDD. BL & /BL is complimentary to each other. Output is also obtained with this Q & /Q is also complimentary to each other with respect to BL & /BL. In my work this circuit is simulated in three technologies 65nm and 90nm. And calculate the power dissipation & Delay with the variations of VDD & Temperature. W-EDIT waveforms are shown in Figure 7.

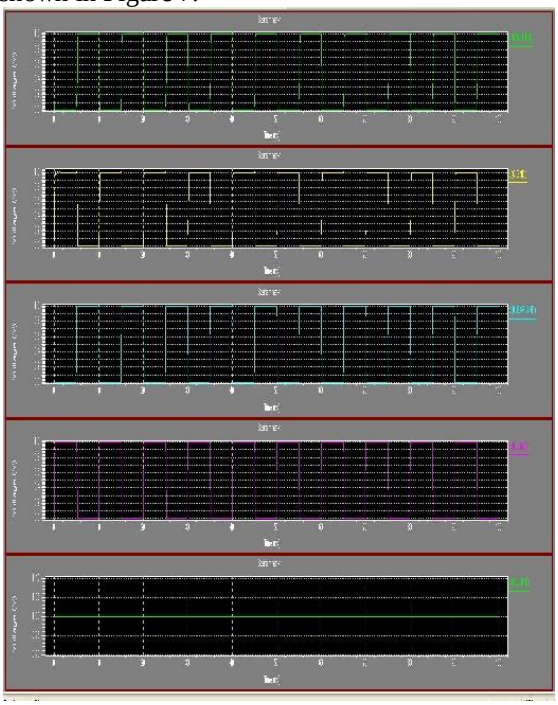
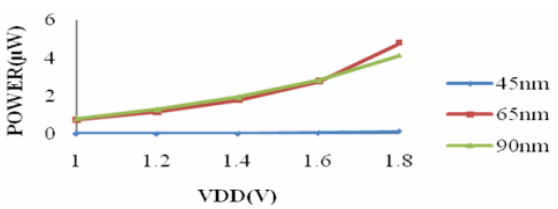


Figure 7 W-EDIT Waveform

III. SIMULATION & RESULTS

Technology	65nm	90nm
VDD(V)	POWER(uW)	POWER(uW)
1	0.756	0.84
1.2	1.175	1.32
1.4	1.792	1.95
1.6	2.765	2.83
1.8	4.814	4.16

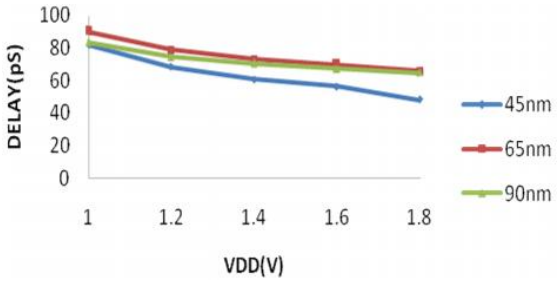
Table 1 Power calculated with the variation of Vdd at 65nm & 90nm technologies



Graph 1 variation of power with respect to Vdd

Technology	65nm	90nm
VDD(V)	DELAY(pS)	DELAY(pS)
1	89.997	83.576
1.2	78.951	74.801
1.4	73.288	70.543
1.6	69.784	67.489
1.8	66.075	65.058

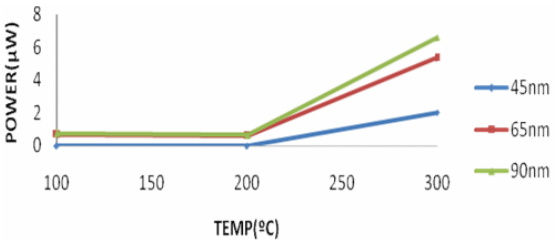
Table 2 Delay calculated with the variation of Vdd at 65nm & 90nm technologies



Graph 2 variation of Delay with respect to Vdd

Technology	65nm	90nm
TEMP(Deg C)	POWER(uW)	POWER(uW)
100	0.714	0.771
200	0.648	0.692
300	5.431	6.649

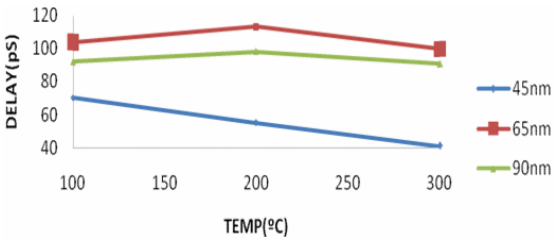
Table 3. Power calculated with the variation of Temperature at 65nm & 90nm



Graph 3 variation of power with respect to Temperature

Technology	65nm	90nm
TEMP(Deg C)	DELAY(pS)	DELAY(pS)
100	103.7	92.32
200	113.4	98.46
300	100.1	90.99

Table 4 Delay calculated with the variation of Temperature at 65nm & 90nm



Graph 4 variation of Delay with respect to Temperature

IV CONCLUSION

Simulation of 6T SRAM memory cell has been performed in TANER EDA Tool. In simulation work, operations were analyzed through waveforms and output files obtained. Results obtained from simulation of 6T SRAM suggests that 6T SRAM cell shows overall least power dissipation in 65nm Technology it takes very small area and consumed least power. In case of second parameter delay it has least delay at 65nm technology. As per our observation we prefer the 65nm Technology because it has low power consumption and highest speed to write data in SRAM Cell.

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