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Analysis of Low power and Small-swing Self-biasing transistor Domino logic

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Abstract*—The proposed novel self-biasing transistor domino logic (SBTDL), SBT acts as smart switch by virtual power gating. The simple approach minimizes the complication while suppressing the leakage current in standby mode. In addition to that SBTDL low output voltage swing reduces the dynamic power dissipation. Whereas recent power gating techniques required an extra circuit and multi-threshold transistors thus increase the complexity in circuit. The proposed design examines through n-input OR gate, 1-bit full adder and cascaded full adders in terms ofleakage power, average power and energy-delay product.Simulations have been performed through BSIM 3.1, TSMC 90 nm technology. 1-bit full adder and cascaded full adders have reduced EDP up to 61% and 60% respectively. The output voltage swing is in between 0.18 V to 1.02 V which is a 70% of full swing.

***Index Terms*—CMOS, domino logic, DSVL, MTCMOS, self-biasing transistor, small-swing**

1. INTRODUCTION

The portable devises generally has longer standby period then the functional period. Therefore, longer standby period consumes extreme power seriously. Dynamic power dissipation measured as the significant source of power dissipation and thus can beminimize up to 70% of the total power dissipation. Dynamic power is directly proportional to the supply voltage and voltage swing[1]. Shrinking the supply voltage significantly decreases the total power dissipation. However, in scaled technology the leakage current has been increasedexponentially.Similarly at thelow threshold and low temperature during long standby periods, most of the power dissipation canarise through sub-threshold and gate oxide leakage current [2-3].As leakage currents become more significant in total power consumption, theindustry need to re-examine the circuit design that restricts system performance, cost and chip size [4].

$$P_{total} = (\propto . C_L . f_{clk} . V_{DD} . V_{sw}) + (I_{SC} . V_{DD}) + (I_{leak} . V_{DD}) \quad (1)$$

Whereas, $\propto$ is the switching activity factor, $C_L$is the load capacitance, f_{clk} is the clock frequency, V_{DD} is supply voltage, and V_S is voltage swing, I_{SC} is short circuit current and $I_{leakage}$ is leakage current. The short circuit current (I_{sc}) occurs directly from the power supply to the ground whenboth the NMOS and PMOS transistors are simultaneously turn on. The leakage current ($I_{leakage}$) are mainly from sub-threshold andtunnelling current. Most of the digital circuits, maximum power is dissipated due to switching activity. Low voltage swing in equation (1) can reduce the dynamic power consumption [5-7].

Dynamic domino logic design has several advantages as compared to static CMOS logic, such as compact chip area and high speed in operation. Hence, the domino logic design has been widely used in system-on-chip design. The leakage power dissipation is become main concern in portable devices when the device is in ideal. Recently, various power gating schemes has proposed to minimize this problem. Some of the standardtechniqueare used, such as multi-threshold transistors [8-9], variable threshold voltage [10], sleep transistor [11], super cut-off CMOS [12], dynamic self-controllable-voltage-level [13], low-swing [14] etc. Sever attempts has been made to eliminate at the cost of high complication design but failed to achieve. Another emergingpower gating technique for leakage power reduction is self-biasing transistor (SBT) [15]. In this method, the power supply is cut off during the idle state thus eliminates the leakage phenomena.

In this paper, Self-biasing transistor domino logic (SBTDL) was proposedto eliminate leakage power and dynamic power dissipation. The SBT gate and drain terminals mergedtogether to works as a current-controlled switch.The proposed circuit examines the impact of SBT on leakagepower and average power dissipation for universal logic gates and cascaded full adders.

2. PREVIOUS WORK

Some of the well-known techniques for reducing leakage current and standby current are MTCMOS, VTCMOS, SVL, DSVL and small-swing technique.

A. Multi-threshold CMOS (MTMOS)

In MTCMOStechnique, high-V_{th}transistors reduce the leakage in standby mode by disconnecting the supply voltage to the PMOStransistor.The unique future of the MTCMOS is that the high and low-V_{th}transistors are in same chip. However, it has serious problems such as the requirement for extra fabrication procedure for high-V_{th} and it is difficult to retain the same data in case of memory circuit design.A low-V_{th} device has lower delay and therefore it switch faster [16]. However, the penalty is that low-V_{th} devices exponentially increasethestatic power and becomes the source of the large standby power. As the portable deviseshas longer standby period therefore longer standby period consumes battery power seriously [17-18].

B. Variable threshold CMOS (VTCMOS)

AVTCMOSscheme eliminates leakage current byvariable the threshold voltage through increasing substrate-bias voltage.The significant problem with substrate bias technique is limited range of V_{th} adjustment. This technique has drawback of very slow operation due to substrate-bias voltage variations, extra supply voltage consumes more power, and it also required large area.This technique is not appropriate for fully depleted and partially depleted SOI process method due to the body of each MOS transistor required to connect for subtract biasing [19-20].

C. SVL technique

A self-controllable voltage level (SVL) design can meaningfully decreases the leakage power consumption in standby mode by dynamically adjusting the supply and ground voltages. The upper and lower part of the SVL circuit consist PMOS and NMOS sleep transistor are switched-on during active mode and switched-off during ideal mode. Moreover, it can successfully retain the data even in long standby mode and it is also suitable for registers and memory devices. This circuit has higher noise margin along with minimal area overhead. [21]. However, SVL design has drawback of leakage current as compared to MTCMOS and SCCMOS design [22].

D. Dynamic SVL technique

The dynamic SVL (DSVL) design has proposed to reduce leakage current in SVL technique by variable threshold voltage using reverse body biasing (RBB) and increasing the voltage drop across the NMOS and PMOS transistors that reduceddrain-induced barrier lowering (DIBL) effect [23]. Combination of this two techniques DSVL design attains low leakage power dissipation throughout idle mode. However, this technique requireadditional transistor for upper and lower SVL power switch. Furthermore,itneeds external bias RBB and FBBand hence, the body bias reduces the performance [24].

E. Small-swing technique

A small-swing technique consist twisted diode connected PMOS and NMOS transistor. These are placed in between pull-up and pull-down network. The twisted connected PMOS and NMOS transistors reduce the output voltage swinghigh to (V_{DD}-V_{th}) depends on the sizes of transistor. Sang-Yun Ahn et al, proposed small-swing domino logic technique to reduce power consumption and this design reduces the output voltage swing up to 70% of the full swing [25].

3. SBT TECHNIQUE OPERATION

A self-biasing transistor has projected to reduce the leakage current in standby period during the ideal mode. The basic purpose of transistor biasing is to keep transistor is in either saturation mode or cut-off mode. Transistor steady state operations depend on its gate and source voltage. The SBT has its gate and drain terminals combined together and which functions as a current-controlled switch. The drain to gate feedback alignment ensures that the transistor is always biased either in saturation or cut-off region irrespective of the supply voltage. The self-biasing transistors are shown in Figure. 1.

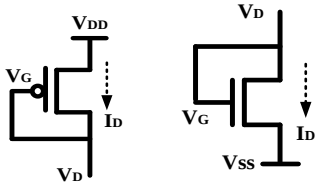


Figure. 1. PMOS and NMOS transistor with SBT technique

The current through a short-channel device and long-channel device in saturation is given by equation (2) and for long-channel device; equation (3) can be used.

$$I_{dsat} = W.v_{sat}.\ C_{OX}\,(V_{GS} - V_T) \quad (2)$$

$$I_{dsat} = \frac{1}{2}k_n(V_{GS} - V_T)^2 \quad (3)$$

Where, v_{sat} is the saturation voltage in short-channel device, $k_n = \mu_n C_{OX}(W/L)$is the process transconductance of the device. For deep sub-micron devices, equation (2) can be rewritten and used to obtain the following equation:

$$V_{GS} = \frac{I_{dsat}}{W v_{sat}\, C_{OX}} + V_{T'} \quad (4)$$

The above equation shows that V_{GS} is proportionate to I_{dsat} for deep sub-micron devices too.Equation (4), can be modified as

$$V_{GS} = \sqrt{\frac{2I_{dsat}}{k_n}} + V_{T'} \quad (5)$$

V_{GS} being equal to V_{DS}, if the current is large, then the gate voltage V_G becomes greater than V_T and the device drives into saturation region.

4. PROPOSED SMALL-SWING SBT DESIGN

Recently many techniques have been proposed and executed for low-power consumption. Main aim of these techniques is to reduce the voltage signal swing level high to (V_{DD} - V_{th}), while maintaining the low voltage level at Gnd. Basic SBTCMOS design has shown in Figure 2.

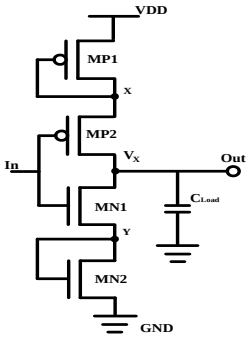


Figure 2. Basic SBTCMOSdesign

In the pre-charge period, the SBT PMOS transistors function in the saturation region and behave as resistors.The resistances of the SBT transistors are denoted as R_{MP} and R_{MN} and their equations are given by

$$R_{MP} = \frac{1}{\mu_p C_{ox}\,(W_{MP}/L)(V_{SG} - |V_{THP}|)} \quad (6)$$

$$R_{MN} = \frac{1}{\mu_n C_{ox}\,(W_{MN}/L)(V_{GS} - V_{THN})} \quad (7)$$

$$t_{pd} \propto \frac{C_L V_{DD}}{I_{DS}} \approx \frac{C_L V_{DD}}{A(V_{DD} - V_{th})^2} \quad (8)$$

Where W is width, L is length of the transistor, $V_{SG}$the source-to-gate and V_{GS}gate-to-source voltages.

The capacitance at node x and node y generated by MP1 and MN2 are$C_x = C_{GD} W_{MP1}$and $C_y = C_{GD} W_{MP2}$ respectively. C_{GD} is the gate-drain overlap capacitance,
Voltage at node Y is

$$V_y = V_{out}\left(1 - e^{-t_{pre}/R_{MN1}C_y}\right) \quad (9)$$

Voltage at node X is

$$V_x = V_0\left(1 - e^{-t_{pre}/R_{MP1}C_x}\right) \quad (10)$$

Voltage at output node is

$$V_{out-high} = V_x\left(1 - e^{-t_{pre}/R_{MP2}C_{Load}}\right) \quad (11)$$

Similarly output low is

$$V_{out-low} = V_y\left(1 - e^{-t_{evel}/R_{MN1}C_{Load}}\right) \quad (12)$$

High and low voltage at output swing is determined by theequation 12 and equation 13 which is correlated with capacitive load and resistancesof the SBT's. As capacitive load increases voltage swing level reduces. Similarly, a resistance is inversely proposal to width of the transistor as width increases resistances decreases. The voltages swing level increases as width of the transistor increases.

To overcome the problem of large power dissipation in domino logic design, SBT power gating transistor has connected in between supply voltage to PMOS and pull-down network to ground. The proposed SBTDL design has shown in Figure 3.

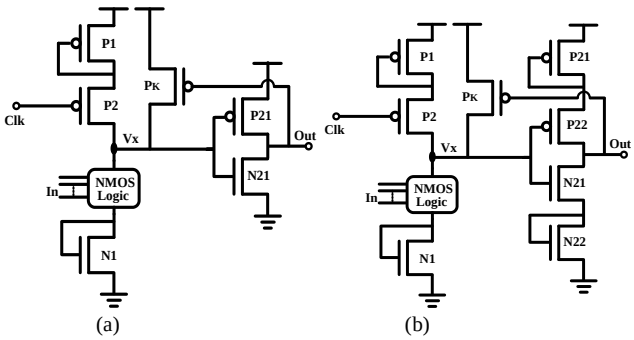


Figure 3.Proposed basic structure (a)SBTDL1 and (b)SBTDL2 design

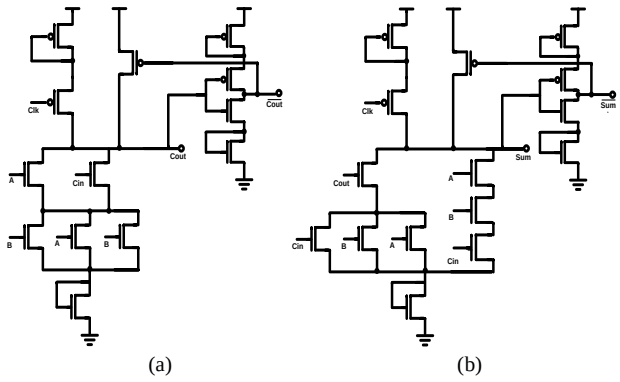


Figure 4. Proposed SBTDL design (a) Carry cell (b) Sum cell

5. IMPLEMENTATION AND SIMULATION RESULTS

In order to evaluate the effectiveness of SBT technique we designed series of inverter with capacitive load, frequency and supply voltage variations respectively, static NAND gate with CMOS family techniques, n-input dynamic OR gate, 1-bit full adder circuit and series of full adders with domino logic techniques. The simulation are carried out through BSIM3.1by TSMC 90 nm technologyspice simulator at V_{DD} = 1.2 V, raise time and fall time of the input pulse is same, capacitive load is 10 fF, frequency is 200 MHz and temperature at 25 °C. Transient analyses are performed 100 ns duration, leakage power has calculated when the input signal is low and the average power is calculated throughout the duration. Furthermore, Power-Delay product (PDP) and Energy-Delay product (EDP) measured to know the efficiency of the design. For all designs comparative results of leakage power and average power dissipation are shown in graphical representation.

A. Series of inverter

The power saving advantage of the SBTCMOS low power design has illustrated through sequence of four inverters. The size of transistor is W/L= 5 for PMOS, W/L= 3 for NMOS, SBT has chosen three time of normal transistor. The percentage of power saving has measured with load capacitance, frequency and supply voltage variations, Table 1 show that the higher capacitive loads has higher power saving. The higher operating frequency leads to increased power saving, similarly low supply voltage has good power saving as compared to conventional circuit and the simulation results are summarized in Table 2 and Table 3.

Table 1: Power saving comparison for different load capacitors in 90 nm technology

Cap. Load (f)	**10f**	**25f**	**50f**	**75f**	**100f**
Conventional	5.0429	7.6364	10.8759	14.2658	17.7331
SBTCMOS	2.6122	3.7791	5.4321	6.5907	7.3602
Saving	48%	50%	50%	53%	58%

Table 2: Power saving comparison for different frequencies in 90 nm technology

Freq. (Hz)	**400M**	**200M**	**100M**	**50M**	**25M**
Conventional	10.2814	5.0429	2.5659	1.3146	0.8059
SBTCMOS	4.5665	2.6122	1.4654	0.8586	0.5787
Saving	55%	48%	43%	35%	28%

Table 3: Power saving comparison for different supply voltages in 90 nm technology

Voltage(V_{DD})	**1.4 V**	**1.3 V**	**1.2 v**	**1.1 V**	**1.0 V**
Conventional	7.3650	6.1018	5.0429	4.1403	3.3916
SBTCMOS	4.3685	3.4298	2.6122	2.0705	1.5193
Saving	41%	44%	48%	50%	55%

B. SBTCMOS performance

Basic building block of universal two inputs NAND gate has chosen to compare SBTCMOS technique with conventional CMOS which is basic, MTCMOS [9], small-swing CMOS (SSCMOS) [25] and DSVL [22] in terms of leakage power and average power dissipation. We sizes the transistor W/L= 5 for PMOS, W/L= 3 for NMOS, W/L= 15 for SBTPMOS, W/L= 10 for SBTNMOS, capacitive load is 10 fF and temperature is 25 °C. Comparative analysis of five techniques leakage power and average power dissipation has shown in Figure 5(a) and Figure 5(b). Simulations result shown that the SBTCMOS design has

achieved better result as compare to all other four techniques, 20% in case of leakage power and 46% in case of average power has reduced as compared to basic circuit. The output voltage swing is between 0.18 V to 1.0 V which is a 68% of full swing. Moreover, SBTCMOS has attained lower PDP and results are as shown in Figure 5(c).

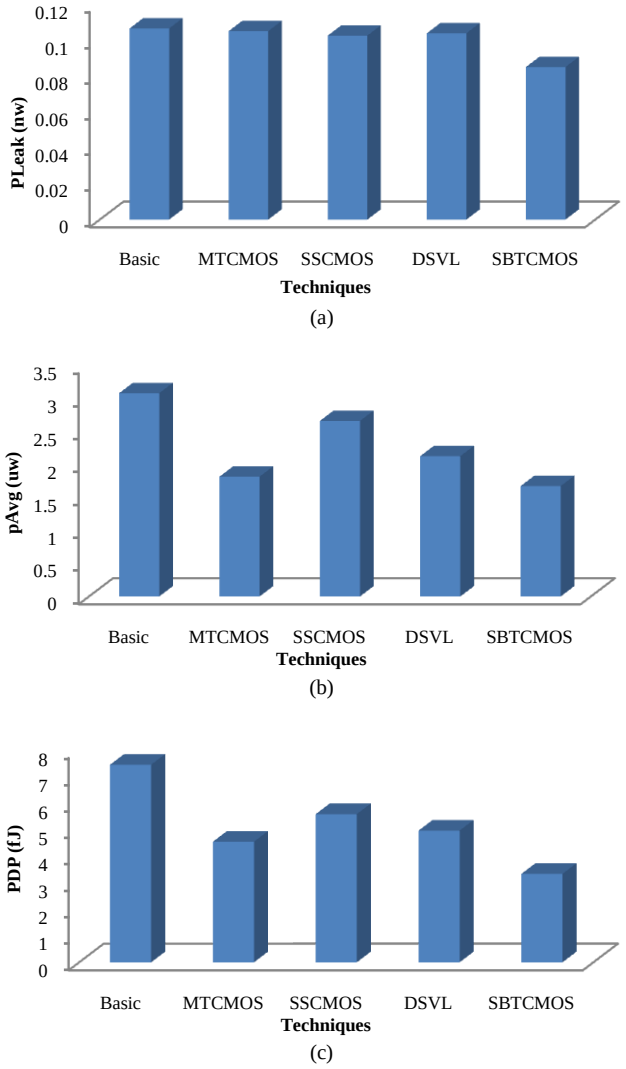


Figure5. Two input NAND design with various techniques (a) leakage power (b) Average power (c) PDP

C. SBT-Domino logic performances

To examine the proposed designs has shown in Figure 3. We designed dynamic OR gate with two, three and four inputs at different V_{DD} and various temperatures. These are compared with Basic domino logic (Basic), Multi-Threshold Domino Logic (MTDL) [9], and Small-Swing Domino Logic (SSDL) [25] in terms of leakage power, average power dissipation and power-delay product. In all the three cases proposed designs has advanced result. Design of n-input OR gate with various techniques, Leakage power, average power and PDP are show in Figure 6. In case of four input OR gate the proposed design SBTDL2, leakage power and PDPhas decreased to 77% and 72% respectively as compare to basic design. The output voltage swing is between 0.2 V to 1.05 V which is a 71% of full swing. In equation (1), dynamic power is propositional to output voltage swing (V_{swing}). The reduced output voltage swing decreases the dynamic power dissipation as compared with the full voltage swing. The proposed designs has minimized the leakage current in standby period while cut-off the power supply and dynamic power has reduced by decreases the output voltage swing. Hence, total power dissipation in the circuit has reduced meaningfully. In addition to that, OR4 gate leakage power has measure at various temperatures and different V_{DD}. Average power and EDP has calculated which are shown in Figure7. The proposed designs SBTDL1 and SBTDL2 achieved 43% and 72% reduction in EDP at 1.2 V as compared to basic. However, SBTs moderates the speed and the reduced swing decreases the noise margin level.

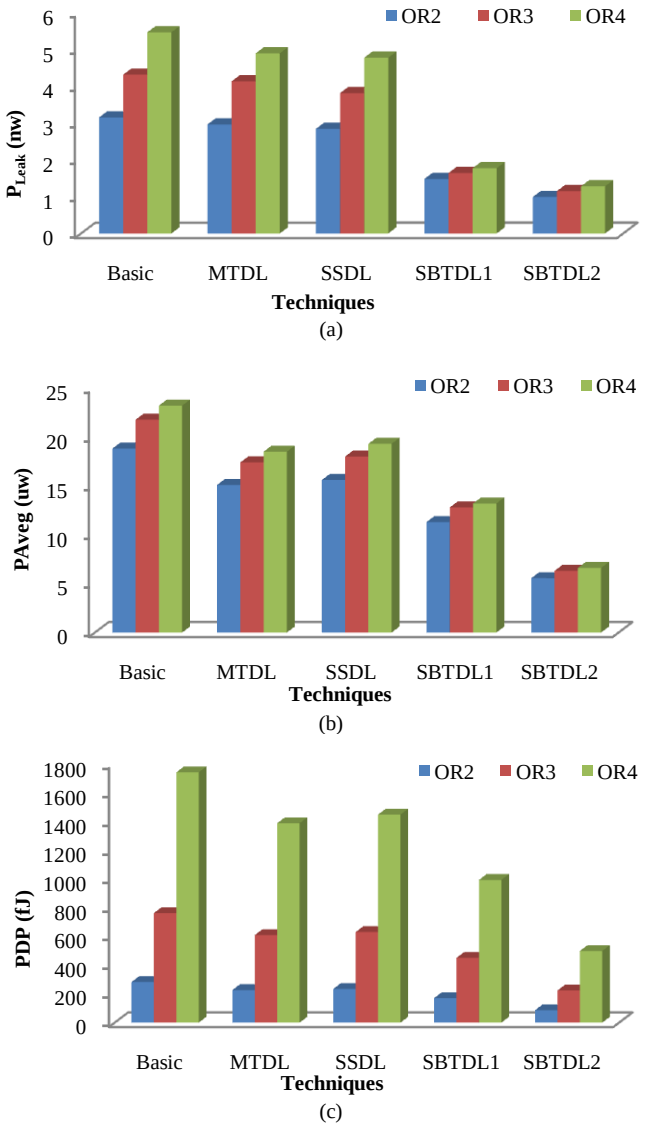
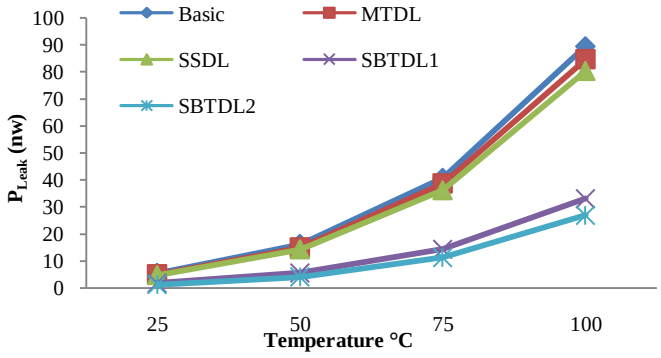


Figure6.n-input OR gate with various techniques (a) Leakage power (b) Average power (c) PDP



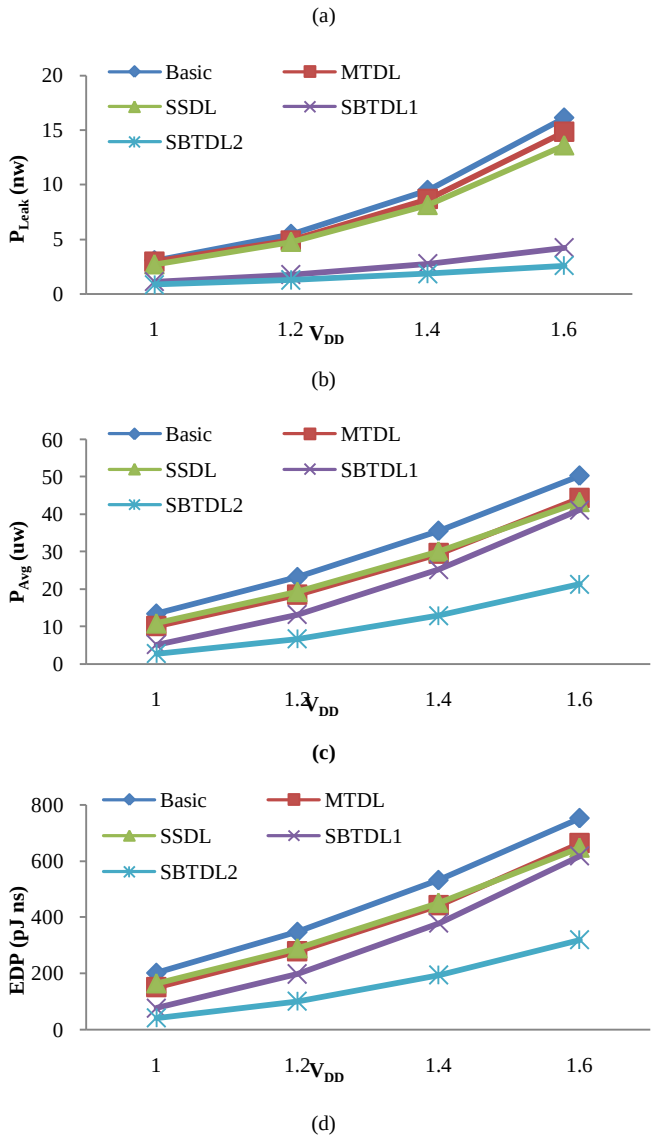


Figure7. OR-4 gate design (a) Leakage power vs temperature. (b) Leakage power vs V_{DD}. (c) Average power vs V_{DD}. (d) EDP versus V_{DD}.

D. Full adder performance

The basic arithmetic 1-bit full adder circuit has shown in Figure4.'A', 'B' and 'C_{in}' are inputs, carry out and sum are the outputs. The proposed design the output voltage swing is in between 0.18 V to 1.01 V which is a 69% of full swing. The SBTDL2 average power dissipation and EDP has decreased up to 63% and 61% respectively. The simulation results of leakage power and average power as shown in Figure 9(a). The EDP has shown in Figure 9(b) which declares that the proposed designs have high energy efficient among all the design.

Arithmatic logic unit consist of cascased full adder cells and each carry output has connected to the carry input of consecutive adder. We designed series of four full adders with various topologies. The SBTDL has low power dissipation along with reduced swing. The new approach, mixed cascading D-FA and SD-FA topology has show in Figure 8. This approach is validate by observering the low power feature of SD full adders with reduced swing, as well as high speed of D-FA with full swing. The mixed D-FA and SD-FA topology has attained low power as compared to D-FA, therefore this approach is well suitable for low power applications. The series of four full adders design average power dissipation and EDP of various techniques are shown in Figure 10.

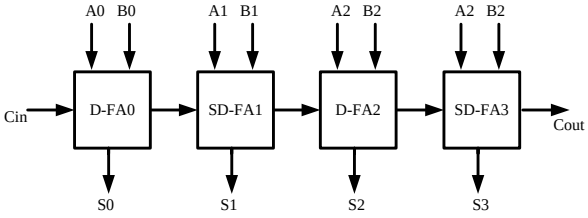


Figure8. Basic block digram of mixed D-FA/SD-FA topology

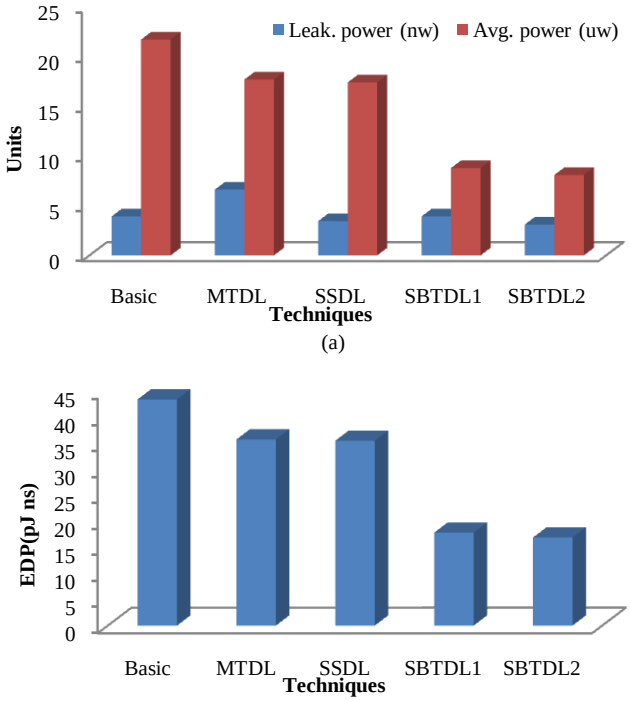


Figure9. 1-bit full adder (a) Leakage power and average power (b) Energy-Delay Product

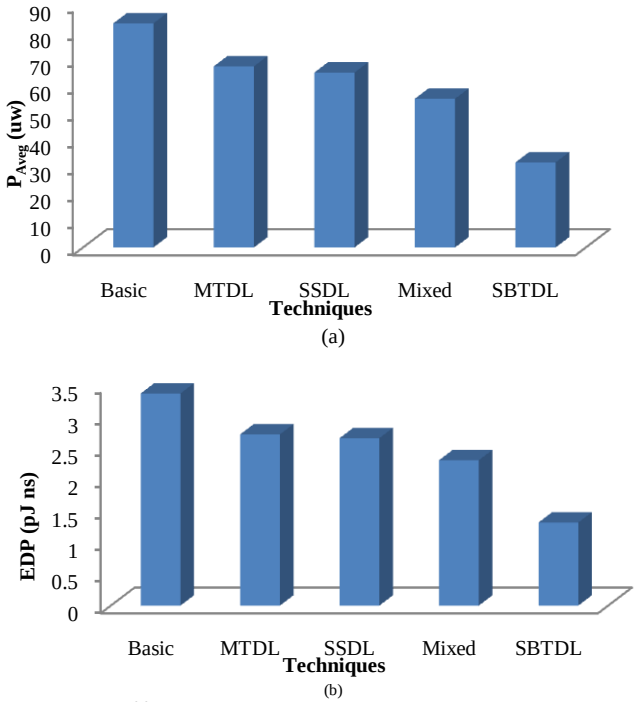


Figure10. Series of full adder design (a) Average power dissipation (b) Energy-Delay Product.

6. CONCLUSIONS

In this paper, SBTCMOS design analysed and compared with other low power techniques such as basic CMOS logic, MTCMOS, SSCMOS, and DVSL. The power saving advantage of the SBTCMOS low power design has illustrated through sequence of four inverters with capacitive load, frequency and supply variations respectively. The proposed SBTDL novel design reduces the leakage power in static mode and dynamic power in active mode.In order to examine the SBTDL technique, basic OR gate with n-inputs, 1-bit full adder and series of full adder's circuits are chosen and compared with recently proposed techniques. The proposed approach achieves better reduction in leakage power and PDP over the basic design. In case of four input OR gate the SBTDL2 design PDP has decreased up to 72%. The output voltage swing is in between 0.2 V to 1.05 V which is a 71% of full swing. Moreover,proposed design 1-bit full adder and cascaded full adder have reduced EDP up to 61% and 60% respectively as compared to basic design. It shows that the proposed SBTDL design is very much effective in energy efficiency, although the design has moderate noise margin. This configurationis well suitable and feasibleto construct digital building blocks and arithmetic logic units.

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