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Design and Implementation of Frequency Synthesizer: A Review

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***Abstract*— This paper focuses on the design of fractional-N frequency synthesizer using PLL which is an important building block in wireless communication. For application where we required small step size for example in situation where almost continuous tuning is required fractional N synthesizer becomes an attractive option. It mainly consist four block: 1) loop filter 2) Phase Frequency Detector 3)Frequency Divider 4) VCO. Fractional Frequency synthesizer using PLL is always preferred as compared to other radio frequency oscillator because of high stability, easy to control from digital circuitry and settling is fast. This review also represent the performance parameter of fractional frequency synthesizer like phase noise, Loop bandwidth and Fractional spur.**

***Index Terms*—Fraction-N frequency synthesizer, Fractional spur, sigma delta modulator, phase noise, voltage control oscillator, frequency divider, 3db loop bandwidth**

I. INTRODUCTION

A range of frequencies is generated from a single frequency and this is done by an electronic circuit which is called as frequency synthesizer. Frequency synthesizer using PLL consist a frequency divider in feedback loop. Fractional N frequency synthesizer have many advantages over integer frequency synthesizer like small step size , higher reference frequency and higher loop bandwidth without compromising the stability of loop. There are many techniques by which we can obtained N division ratio. A conventional technique to achieve fractional N-division ratio is dual loop synthesizer but in this review paper to get better performance Delta-sigma modulator is used for getting N- division ratio. In this review paper section II consist the literate review , section III consist circuit design in which block diagram of fractional frequency synthesizer is described , in section IV performance parameter of frequency synthesizer (3db loop bandwidth, fractional spur etc) is explained, section VI describes the future work and last sectional VII consist result and conclusion in which a comparison table is represented between integer frequency synthesizer and fractional N frequency synthesizer.

II. REVIEW OF LITERATURE

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Tom AD Reliy *et al.* [2]: have discussed various have discussed comparative study of different PLL frequency synthesizers and application area of different Frequency synthesizer. And find that fractional –N synthesis is dominant architecture.

Emad Ebrahimi *et al.* [3]: have discussed frequency synthesizer using using nested PLL. In this paper various sub block have proposed for 65nm CMOS technology. And also gain in forward loop to make the system stable.

Ming li *et al.* [4]: have proposed Fractional –n frequency synthesizer for FSK synthesizer. In this paper various subblock have proposed for 0.18µm CMOS technology and has been realized phase noise -12.96dBc/HZ@1MHZ.

B.Floyd *et al.* [5]: have discussed the advantages of a wide lock range and low phase noise quadrature Frequency synthesizer in wireless communication systems. The quadrature Frequency synthesizer implemented in IBM 0.13µm and provides output power at 50ohm load.

Pallavi *et al.* [17]: have discussed the implementation of integer N frequency synthesizer using phase lock loop. Here integer N frequency synthesizer is implemented in 250nm CMOS technology. This paper also provides a brief introduction of basics of PLL.

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III. CIRCUIT DESIGN

In this review paper Fig:1 show the architecture fractional –N frequency synthesizer which consist PFD/CP,loop filter, VCO(voltage control oscillator) and sigma delta modulator.

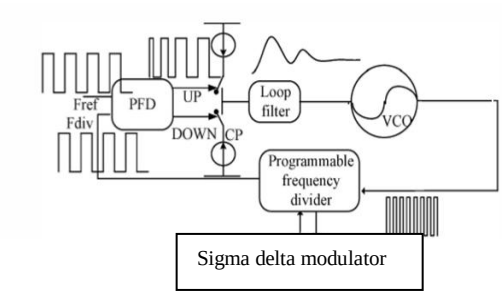

Fig.1 Architecture of fractional-N frequency synthesizer

A. Phase frequency detector and charge pump

A circuit which detect phase and frequency is called PFD. Fig.2 is circuit of phase frequency detector and charge pump PLL. As shown is fig. 2 phase and frequency detector with two current sources with switch s1 and switch s2. Depending upon logic input the current source pump charge in to or out of filter. The circuit works on three states: 1) Qref=Qd=0 then both switch s1 and s2 switches off alternatively and output (Vout) at this state remains constant 2) Qref=1(high) and Qd=0(low) then I1 charge Cp 3) Qref=0(low) and Qd=1(high) then I2 discharges Cp. Now suppose that Qref leads Qd then Qref produce pulses continuosly and Vout arises regularly which is known as up and down current. Here I1 and I2 nominally equal. Fig:3 shows the output waveform of phase frequency detector with charge pump PLL.

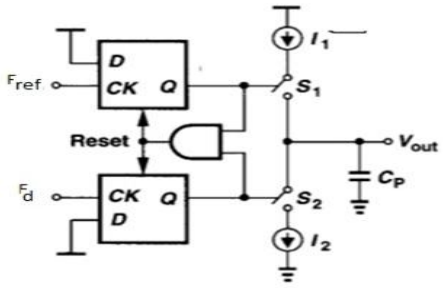

Fig.2 Circuit diagram of phase frequency detector with charge pump

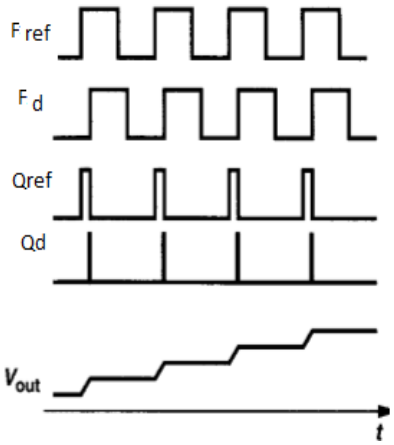

Fig.3 output of PFD with charge pump

Loop filter convert the current from charge pump in to voltage and also work as low pass filter. In fractional N frequency synthesizer, loop filter remove the unwanted component frequency component from the output of phase frequency detector. Here loop filter is second order low pass filter .The output voltage of loop filter is input of VCO or we can say that oscillations of VCO depends upon output voltage of loop filter control . Thus output of loop filter affects various parameter like stability , phase noise and loop bandwidth etc . Fig:4 shows the second order low pas filter. Frequency synthesizer. And find that fractional –N synthesis is dominant architecture

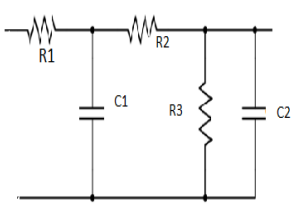

Fig.4 second order low pass filter

C. VCO (Voltage Controller Oscillator)

VCO is most important component in frequency synthesizer .It is a oscillator in which input voltage controls the oscillation frequencies.VCO has large tuning range as compared to other oscillator but it has low Q (quality) factor, hence it consist more jitter as compared to other type. In this review paper ring VCO is used because ring VCO have small chip area, low cost, good performance and easy integration. Ring oscillator is made up of many delay stages where last stage is feedback to first stage as shown in Fig.5. Ring oscillator must provide the 2π phase shift with unity gain to obtain the oscillation. Single ended ring VCO is shown in Fig.5 and Schematic of delay cell is shown in Fig:6 Here primary loop is formed by M1 and secondary loop is formed by M7 and M8. The output of previous stage is primary input and output of few stage prior to current stages are secondary input. PMOS load transistor M3 and M4 form a latch whose strength affects the oscillation frequency. Feedback strength of latch is control by control voltage Vc at the gate of NMOS transistor M5 and M6.

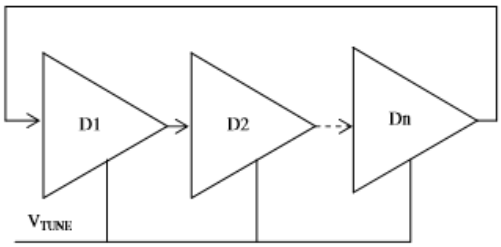

Fig.5 Single ended Ring VCO(voltage control oscillator)

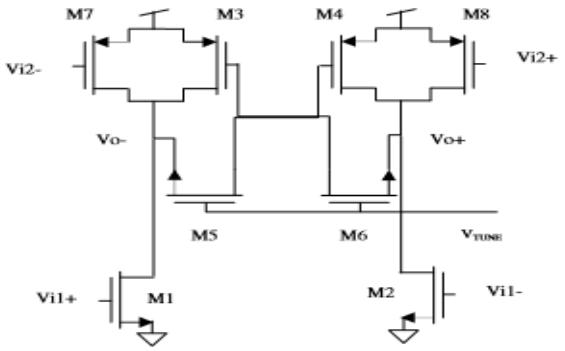

Fig.6 schematic of delay cell

D. Frequency Divider

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Fractional –N division ratio is accomplished with the help of programmable divider to achieve programmable division , sigma delta modulator is used. The main advantage of using modulator is that it does not have a phase noise spectrum because of noise shaping property of modulator Fig.7 shows the detail of second order sigma delta modulator. Function of delta sigma modulator and accumulator is very similar. The only difference between the modulator and accumulator is that accumulator produces 1's and 0's stream while delta sigma modulator generates +1's and -1's stream with + output range .

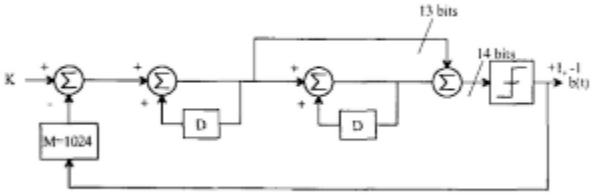

Fig.7 second order delta sigma modulator

IV. PERFORMANCE PARAMETER

A. Fractional spur

In fractional –N frequency synthesizer; spurs are produced at output of VCO and behaviour of these spurs are depend upon the feedback Divider (programmable divider) whose value is switch between two different integers to get a fractional number. The fractional division ratio M_f will be given as:

$$M_f = \frac{K(M+1)+(N-K)M}{N} \quad (1)$$

Here N is a Division modulus and division by M+1 is chosen K times and division by M is chosen N-K times.

Magnitude of Kth spur harmonic Vsk is defined by equation

$$Vsk = \sum_{-\infty}^{\infty} j_{k-m}(\alpha 1) j_m(\alpha 2) \quad (2)$$

Here α1 and α2 is defined as

$$(\alpha 1) = 2\pi Kvco\frac{V1}{Ws} = V1\ Kvco/Fs \quad (3)$$

$$(\alpha 2) = 2\pi Kvco\frac{V2}{2Ws} = V1\ Kvco/2Fs \quad (4)$$

Ws =2πFs; Fs is spur frequency and Vi is defined as i-th harmonic amplitude and Kvco is sensitive parameter of voltage control oscillator. Frequency of spurs be conditional on two parameter one is Division ratio of feedback and other one is lowest frequency which is given by f_{ref}/N .

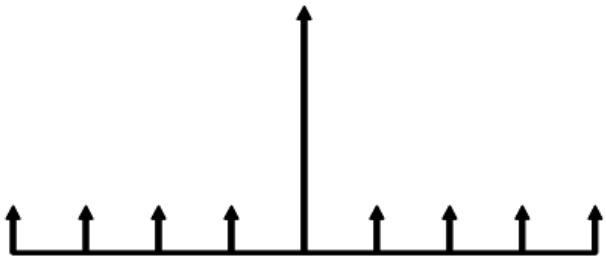
Fig.7 reference side band (spurs)

Now to reduce the spurious sideband we should reduce the f_{ref} with loop bandwidth and this can be done by using higher order filter. Also by reducing the leakage current, spurious sidebands can be reduced.

B. Bandwidth

The loop 3db bandwidth taken in to account for study of noise. The loop 3db bandwidth is determined by w_n and ζ where wn and ζ are natural frequency and damping constant respectively. The loop 3db bandwidth is given as:

$$w_{3db} = w_n[1 + 2\zeta^2 + \sqrt{(2\zeta^2+1)^2+1}]^{1/2} \quad (5)$$

$$w_{3db} = 2w_n \text{ for } \zeta = 0.707(\zeta < 1) \quad (6)$$
$$w_{3db} = 2.5w_n \text{ for } \zeta = 1$$

C. Phase noise

Phase noise of a frequency synthesizer based on PLL is very important parameter because it effects the performance of system specially if it is used in radio communication application. Phase noise is also known as phase jitter. Practical all the signal sources produce some phase noise or phase jitter. If we are assuming PLL (phase locked loop) is a LTI (linear time variant) system then we can calculate the total phase noise as:

$$Q_{no}^2 = N^2(Q_{nr}^2 + Q_{neq}^2) + (\frac{O(s)}{1+O(s)})^2 + Q_{nv}^2(\frac{1}{1+O(s)}) \quad (7)$$

Where Q_{neq}^2 is given as:

$$Q_{neq}^2 = \frac{1}{K_d^2}(Q_{np}^2 + Q_{nl}^2) \quad (8)$$

Here Q_{nr}^2 is reference phase noise,Q_{nv}^2 is VCO noise, Q_{np}^2 is PFD (phase frequency detector) noise and Q_{nl}^2 is LPF phase noise.

$$\frac{O(s)}{1+O(s)} = \frac{\frac{K_d K_o F(s)}{N}}{S + \frac{K_d K_o F(s)}{N}} \quad (9)$$

Here O(s) is open loop gain which is given as:

$$O(s) = \frac{K_d K_o}{N_s} F(s) \quad (10)$$

Therefore to reduce the total phase noise keep the loop bandwidth as large as possible.

D. Lock in range

When reference clock of PLL and feedback of PLL is matched then, The PLL is said to be matched. Initially PLL is not in lock. Let us consider that reference frequency or input frequency is given by w_1 and output is working at center frequency w_o . In the lock in process output frequency is function of VCO (voltage control oscillator) w_{vco} . Hence initially offset of frequency is given as:

$$w = w_1 - w_0 \quad (11)$$

The lock in range is defined as:

$$w_l = K_{vco}K_{pd} + 2\pi R \quad (12)$$

From the loop gain of charge pump PLL we get $2\zeta w_n = \frac{K_{vco}K_{pd}R}{N}$

Hence the lock in range is given by :

$$w_l = 4\zeta w_n \quad (13)$$

E. Switching speed

In a frequency synthesizer , the switching speed is the amount of time(period) at which the instruction is requested for the succeeding frequency before the time at which the output of synthesizer become practicable and conditions are met .The switching speed is also termed as switching time or settling time.

A more general wording has been provided by James A. Crawford is that 50 reference frequencies of 50 KHZ has a switching time of 1 millisecond [19]. And two other author state that switching time (settling time) depend upon percentage change in feedback division ratio [20]. Settling time of a second order system is given as:

$$T_s = \frac{4}{\zeta w_n} \quad (14)$$

F. Step size

Suppose the N is a loop division and is a fractional number also that is N is given by:

$$N = K / f \quad (15)$$

Here variable K and F are the integer numbers.
Now the least step size is given as:

$$\text{Step size} = \frac{f_r}{f} \quad (16)$$

Here f_r is reference frequency or input frequency and by using above equation the step size can be reduced without reducing the reference frequency.

G. Power consumption

In VLSI (Very large scale integration) low power consumption is biggest challenge. Low power consumption has many advantages; for example the main advantage is that it reduce stringent cooling requirements and it result in inexpensive and more compact product [20].

Loop filter which limit the switching time or switching speed between cycle and sigma delta modulator which is used to remove the noise produced by loop filter are the major sourcr for optimization of power.

V. FUTURE WORK

In newer system design, Integrated VCO and PLL modules will be significant growth in newer system designs. And also board area and cost is important parameter of design of an initial design .the future block of multi-standard high-data rate wireless system of architecture of

local oscillator is dominated by the super fast lock times, versatility inherent and phase noise improvement.

VI. RESULT AND CONCLUSION

Fraction –N frequency synthesizer using PLL can be easily integrated, consumes power and less area as compared to other synthesizer and also have better noise performance as compared to integer frequency synthesizer. And has relatively faster switching but main problem or we can say that main disadvantage in fraction –N frequency synthesizer is fractional spur and also produce some quantization noise but this quantization noise can be reduced by using sigma delta modulator.

Table I : show the comparison between integer and frequency synthesizer

Parameter	Integer Frequency synthesizer	Fractional N frequency synthesizer
1)Divide ratio	An integer number	A fractional number
2)Step size	Large(equals to reference frequency)	Small
3)Division circuit	Fixed	Programmable
4)Switching	Slow switching	Faster switching
5)Loop bandwidth	Narrow	Wide
6)Fractional spur	Not presented	Presented
7)Frequency resolution	High	Small

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