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Design and Implementation of Digital Phase Lock Loop: A Review

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***Abstract*— The Digital Phase Lock Loop represent the advancing of PLL. Digital Phase Lock Loop (DPLL) with four main blocks 1) Phase and Frequency Detector (PFD) 2) Voltage Control Oscillator 3) Loop Filter 4)Frequency Detector . The DPLL used for wireless communications & feedback is mainly used in DPLL to improve a phase noise and maintain its stability. Clock circuit is important in various audio, video (communication mainly) to store data synchronized. DPLL mostly used for mixed signal solution. Other various applications include jitter reduction, clock recovery, clock generation, and clock multiplier. Clock signal use for maintain data synchronization and reduce skew.**

***Index Terms*— Simple PLL or Digital PLL, PD (phase detector) filter (loop filter), VCO(voltage control oscillator), Amplifier.**

I. INTRODUCTION

PLL consist a feedback system that estimate output phase to input phase. It consists of phase detector, loop filter and & VCO. The PLL having different types such as simple PLL charge pump PLL, Digital PLL, and All digital PLL. In this case of simple PLL it is simple in structure and having components such as Phase detector, and VCO. But some ripples or some noise is present so we use a LPF in between the Phase detector and VCO. Some problems are occurs in the simple PLL that is acquisition range problem. To remove this problem we are using the charge pump PLL. In this Charge Pump PLL we are using a D flip flop in place of simple phase detector, loop filter and VCO. The charge pump PLL increase the stability of system and also performance. IN this simple PLL and charge pump PLL all the components are of analog type but In this case of Digital PLL the Phase detector is of digital type but the loop filter and VCO is analog type and in All Digital PLL all the components are of the digital type so it is called the ALL Digital Type PLL. In Digital PLL it is also a feedback device and using frequency divider in feedback. DPLL commonly use in communication (wireless communication, wireline communication). Its having advantages such that less power consumption, less leakage current, require less supply voltage. Due to this low power, small area causes quantization noise less which causes degradation in the jitter reduction. If circuit latency decreases then we achieve good jitter reduction.Generally PLL used in frequency modulation whose changed frequency obtained from VCO output when PLL locked. Application of DPLL in FM radio rx. at a frequency divider and also generate clock. The DPLL have 2 external components 1) DAC 2)VCO . In digital PLL, resolution and DAC speed are considered for performance. DAC helps in DPLL, from this resolution is increased quantization noise decrease. & jitter reduction decrease. Speed of DAC is controlled by slew rate of output voltage. We require the gain should be as low as possible for design requirement as reduction in gain reduces the effect of DAC resolution rate. When DPLL having low B.W(bandwidth) then the output noise of PLL is same as the Intrinsic noise of VCO. Some other problems also come in this case of DPLL such as some non linearties will present in the circuit and there are some impractical results present frequency divider.

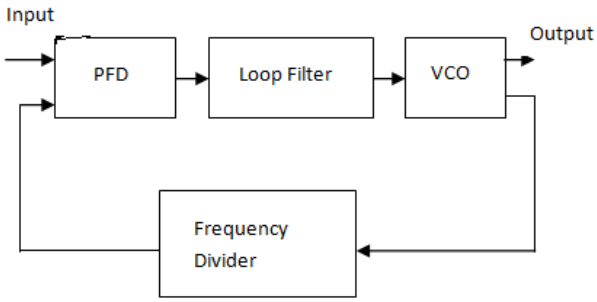

Fig.1 Block diagram of DPLL(Digital phase lock loop)

In this review paper section II consist the literature review, section III describes the literature review , section describes the design of DPLL in which every block of DPLL is described, section IV consist the implementation of DPLL, in section V application of DPLL are described ,section VI describes the analysis of phase locked loop and last section VI consist conclusion in which comparasion table between simple PLL and digital PLL is described.

II. REVIEW OF LITERATURE

Chih-Lu Wei and Shen-Iuan *Liu et al[1]:* has discuss about the improving of phase noise of digital phase lock loop. The Digital PLL is fabricated in a 40nm CMOS process. This paper also describes the various applications such as wireless

and Wireline communications. DPLL may also have a disadvantage it also consume lot of power and area. The Power consumption is 3.51mW at a1.1-V supply voltage.

Jijie Wei Yan Peng Ge Yu *Liu et al[2]:* This paper describe the verification of DPLL using the space Ex Hybrid-system tool. This also show about the non linear transfer functions, quantization error and other non idealities. In this case standard commercial CAD tool such as spectre @ from cadence. A limitation of the Space Ex based approach is that the model parameter of piece-wise linear inclusion are fixed.
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Andreas Winterstein, Achim Dreher *Liu et al*[3]: This paper describe the technique for the communication system. In this paper show a digital implementation of retro-directive receiver to be realized on FPGA here describe the phase detection and performance and also noisy input signal.

Bin Zhao,Dan Lei Yan *Liu et al[6]:* This paper proposed for the 2.4G wireless communication applications. The PLL is designed and fabricated in 0.65µm CMOS process and the whole digital block area is 0.065mm2. In this proposed circuit noise reduction of the quantization noise that caused by metastability between the reference clock and the DCO output clock.

Justin Gaither *Liu et al* [7]: has discuss about the jitter reduction, clock multiplier, clock recovery clock generation and also for the data synchronization. DPLL utilizes spare resource in a Virtex-4 FPGA and require minimal externa components. In this the test result shows very low noise and ability to lock to and filter noise. This paper describe most effective for the first order and second order for the gain constant. This design effective for the video and communication.

Keita Arai and Cong-Kha Pham *Liu et al* [8]: has describe the synthesis of frequency using successive approximation (SAR) algorithm. This proposed PLL is designed using 65nm CMOS Process. The number of clocks to lock-in is 10 clocks in the best case and 34 clocks in the typical case. This consumes small area, low power and improves circuit performance.

III. DPLL DESIGN

DPLL contain the basic building blocks such as PFD (phase and frequency detector), RC Loop Filter, VCO, Frequency Divider etc. DPLL design different from analog because frequency Divider introduced delay and phase comparator introduced the non-linear effects.

A. Phase and Frequency Detector

PFD contain D latch which works at rising edge. At D latch input, vdd and clk input signal are given, output is given at frequency divider, and dc lock is synchronized with input. Digital phase detector is used to reduce phase diff. between 2 signals (v1 & v2).

Double edge trigger (d-ff) is used to reduce power dissipation and by this way 33% of power dissipation is reduced. It uses negative feedback signal and digital signal only. PFD interfaces with v1 & v2 and also with freq. to remove noise. In case of phase detector Ex-OR gate is used, which compares VCO signal and input signal (ref. input signal) .Lower and higher frequency components are obtain from output signal. Phase limitations (-90,90) (it is a disadvantage) also exist, because the edges signal edges does not sense by this Ex-or gate output.

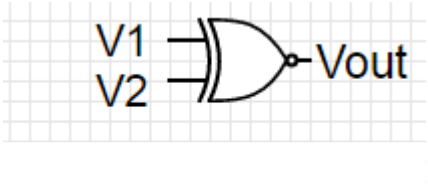

Fig.2 Symbol of EXOR

The difference of frequency modulator output and input is called phase error obtain at the output.

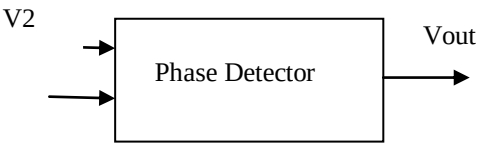

Fig.3 Block Diagram of PD (Phase Detector)

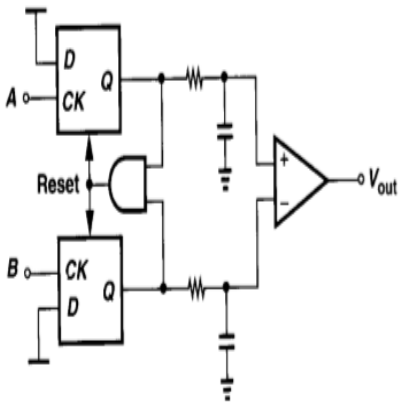

Fig.4 PFD followed by Low Pass Filter

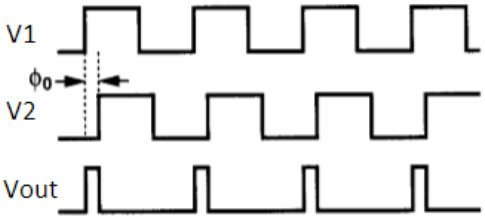

Fig. 5 Waveform of phase Detector

B. Filter

The Loop filter is filtered the phase difference that set the frequency in the feedback. Generally it is RC low pass filter or we say an integrator having a resistance of 30Ω, capacitance of 100pF & frequency of 3db at 53khz. It keeps the loop lock & consists of two separate gain path of 16 bit.
a) Ctrl 8 bit digital control beta: 1st order path which the control small change in phase.
b) Control 8 bit digital control alpha: 2nd order path which maintains the DC bias and tracks the slow and large changes in frequency.

Amplifier: The amplifier is also use in between loop filter and VCO. The amplifier amplifies the voltage, adjust gain or allows adjustment in DC voltage obtained from the output of filter circuit. The unity feedback amplifier is also use.

C. VCO (Voltage Control Oscillator)

VCO is simple voltage controlled oscillator whose output frequency controlled with respect to input voltage. It is having good control and hold range. VCO provides clk circuitry for block in design. It adjust the frequency with the help of PLL and filter. VCO is similar to ring oscillator whose frequency of oscillation controlled by current with the help of inverter .The inverter connect in parallel to oscillator with 2 tri state inverter in which one is enable at a time and another is disable at that time. The capacitor is used in output to reduce frequency. The VCO show locking behaviour in PLL. To support the dynamic v-f(voltage frequency) power down modes (these two are power management technique) the PLL oscillator requires that start-up and change lock frequency should be the 10-100 of time/s.

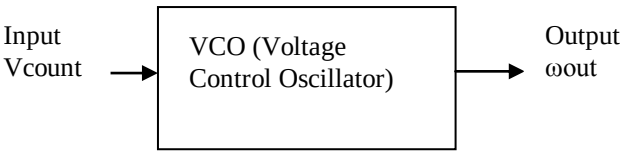

Fig.6 Block Diagram of VCO

$$\omega \text{ out} = \omega 0 + KVCO \text{ Vcount} \quad (1)$$

Where ω0 represent the frequency at which the Vcount=0 and KVCO is the gain or sensitivity of the circuit.

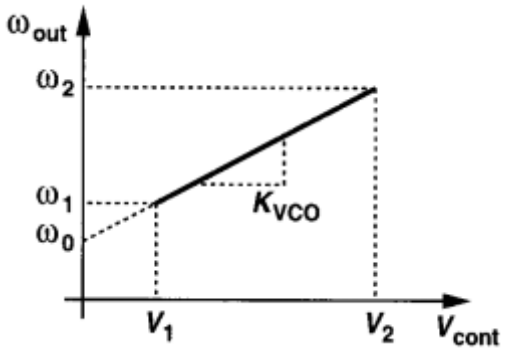

Fig.7 Waveform of VCO

The Vcount is allowable range from v1 to v2 (0-vdd) and tunning range should be atleast ω1 to ω2 then KVCO satisfies this equation.

$$KVCO \geq (\omega 2 - \omega 1)/(v2 - v1) \quad (2)$$

As we increase the tuning range the supply voltage should decrease and the VCO becomes more sensitive to the noise.

D. Frequency Divider

This divides the VCO output frequency that feed to input of PFD. This is called dc lock signal which synchronizes with input signal. It consists of 4-bit synchronous Counter, EX-nor gate, that is activated with the input signal & 4 bit NAND gate.
NAND gate also connected to D-FF that works on falling edge of clock that clear the Counter. The frequency divider show %N in any diagram. The output is N times the VCO output.

IV IMPLEMENTATIONS

This describes two types of implementations of Digital PLL using Accumulating Bang-Bang PD(Phase Detector),Frequency Detector.

A. Accumulating Bang-Bang PD (Phase Detector) (ACBBPD)

It is mainstream implementation and works in most of applications such as jitter reduction, clock and data recovery, clock multiplication.
Reference / input signal will be data signal and the clock signal that must be least half of VCO clock rate. Loop filter use to control BW & stability.

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The operating parameter are such that at which circuit works

- β < α3
- If α, β large then BW decrease & lock time increase
- β < 8
- VCO clock < maxi. S.clock frequency.

B. *Frequency Detector*

In case frequency detector the Counter clock is operated by over sampling CDR, when the Accumulating Bang-Bang PD is not working. PD detects which counter accumulating clock phase more then other. Bit select (programmable) select during loop operation. DN counter bit provides the fast acquisition & UP counter bit result in more immunity.

V. APPLICATIONS

Digital PLL (Phase lock loop) used for digital communication, mobile applications for high speed clock, electronic devices such as hard disk drivers, RF and wireless and optical receivers**.** It also used for jitter reduction, noise reduction & frequency tracking. In this jitter reduction when any random binary signal given to input that effected by jitter due to crosstalk on chip, electronic noise due to components or devices, Parasitic capacitance. To reduce that jitter we add clock recovery circuit (CRC) at the input of signal. IN the CRC circuit the clock produced from the data that reduce the effect of jitter at the input.

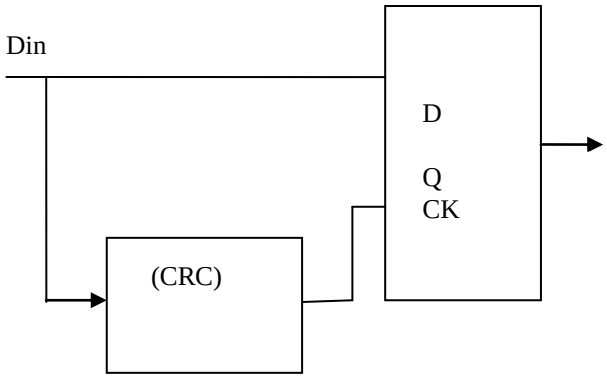

Fig.8 Block Diagram of PLL with CRC

DPLL use for frequency synthesizers & clock recovery. In this case the output is M timer multiple of the input (fout = MfREF) but we need that the output is same as the input (fout =fREF). To reduce that factor (M) we use the frequency synthesizer that stable the output of VCO.
DPLL use to reduce skew. In this case there is a difference between the input signal and output signal that difference is called skew. To reduce or eliminate that skew use of Buffer at output.

DPLL use in FSK Decoder. In this input given to circuit the loop lock the input and then track the input frequency into 2 possible frequencies with the DC shift at output.

VI. ANALYSIS

The DPLL is a linear discrete time model. The main sources of noise in the DPLL are TDC (time to digital converter) which is use in PFD ,clock and filter. The quantization noise is produced by the time to digital converter, phase noise produced by reference clock and also phase noise by the Decimation filter. The TF(transfer function) (Hfilter) of the filter and DLF is

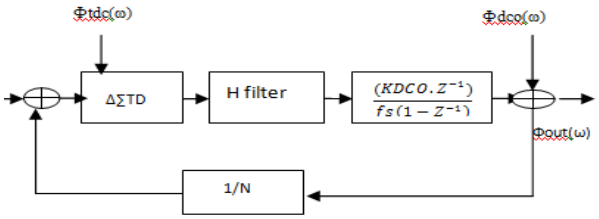

Fig.7 Discrete time linear model of DPLL

$$Hfilter = \left(1 + e^{-j\omega Ts}\right).e^{-j\omega Ts}.Df + \frac{KFIR}{16}.\frac{K1.e^{-j\omega T'}}{1-e^{-j\omega T'}}.e^{-j\omega Ts}. \quad (3)$$

$$KFIR = 1 + e^{-j\omega Ts} + e^{-2j\omega Ts} + \quad e^{-3j\omega Ts} \ldots + e^{-15j\omega Ts} \quad (4)$$

Where the Df is latency of decimation filter of DCO.K1 is integral gain, D1 is latency of DLF to DCO. The OLP(open loop gain) of DPLL is

$$Gloop(j\omega) = Ksh.GmSTF.Hfilter.\frac{KDCO.e^{-j\omega Ts}}{Nfs.(1-e^{\backslash}-j\omega Ts)}. \quad (5)$$

The TF of quantization noise and DPLL O/P is

$$HTDC(j\omega) = \frac{N.Gloop(j\omega)NTF}{1+Gloop(j\omega)STF} \quad (6)$$

The TF of reference clock and DPLL O/P represented as

$$HREF(j\omega) = \frac{N.Gloop(j\omega)}{1+Gloop(j\omega)} \quad (7)$$

The TF of DCO phase noise and DPLL O/P is

$$HDCO(j\omega) = \frac{1}{1+Gloop(j\omega)} \quad (8)$$

The PSD (power spectral density) of total O/P phase noise is

$$Sout(j\omega) = |HTDC(j\omega)|^2.STDC(j\omega) + |HREF(j\omega)|^2.SREF(j\omega) + |HDCO(j\omega)|^2.SDCO(j\omega).$$

(9)

Table.I shows the comparision among simple PLL, Charge pump PLL and Digital PLL

Simple PLL	Charge pump PLL	Digital PLL
Use of analog as well as digital signals.	Analog and digital signal both are use.	Only digital signal is use.
Limited acquisition range problem.	Here this problem is not present.	Also in this PLL this is not present.
Area acquires less	Area acquires more	Here area requirement is less
Analog components are used	All components are analog type	The phase detector is digital type and other are of analog type
Stable	More stable as compare to simple PLL	Stable
Low performance	High performance	High performance
Skew or phase difference more	Skew is reduce	Less phase difference

VII. CONCLUSITION

In this paper general DPLL has been discussed along with its different blocks with their feathers. In DPLL the noise is improved as compared to previous design so we say the design having low noise & better hold and lock (control range). The DPLL synchronise only digital signal. The DPLL commonly use for radio rx & some other communication (wire line or wireless) system.

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