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Dynamic Power Reduction of VLSI Circuits: A Review

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Abstract: **Today's time is demanding for low power architectures. In earlier times power was considered as secondary factor as the designers were concerned about the primary factors like size cost and throughput. But as the technology advancing need for low power devices is increasing hugely. There are various kinds of powers that are dissipated by the circuits. But Dynamic Power dissipation is the most affective part that degrades the performance of any circuit. In this paper Dynamic power Reduction is presented for low power VLSI (very large scale integration) circuit design is taken into account . Various techniques have been studied to optimize the dynamic power dissipation like reducing chip area, advanced interconnect , supply voltage scaling, better design techniques, appropriate power management strategies .**

Index Terms **: VLSI, Low Power Design, Power Dissipation, Dynamic Power, Clock Gating etc.**

I. INTRODUCTION

The rate of dissipating the energy from the source to the system over a time is basically referred to as power dissipation. It is basically classified into two categories:1.Peak Power 2.Average Power Maximum instantaneous power over a time is known as Peak power which makes the device less reliable by introducing the glitches due to which the system may not work properly. Cooling and packing of the system are affected by average power. Reducing power consumption is an engrossing area in very large scale integrated circuits (VLSI) design. Most of transportable devices accessible in the marketplace are derived by battery . These devices obtrude solid limitation on power dissipation. Reducing power consumption in these devices enhances battery life remarkably. Due to menial betterment in battery technology, low power design has become more exigent research area.

In this review paper section II consists of Literature Review, section III consists of basics of Power Dissipation, section IV consists of Sources of Power Dissipation, Section V consists various Dynamic power reduction techniques, section VI consists of Why Low Power, section VII consists of various Performance Parameters, Section VIII consists of Future scope, Section IX consists of Conclusion.

II. LITERATURE REVIEW

Mr.Suhas D.kakde *et al.[3] have* proposed the different low power design strategies.And also provided the different factors to reduce the switching activity. And also realized that low power interconnect using advance technology reduced swing or reduced activity approaches.

Sung-mo kang *et al* , [1] have described the need of low power design and also proposed the different methodology to achieve low power consumption.This chapter has primarily concentrate on the circuit –or transistor-level design .

Gary Yeap , [2] have described different technique to reduce the leakage and static current, switching voltage, capacitance, switching frequency and find out several popular figures of merits for low power design.

Kamal K Mehta, [9] have covered literature review of dynamic power dissipation aspect and related technical issue. And also elaborated various factor to reduce power dissipation. This paper discuss about residue effect on system design after dynamic power problem is incorporated.

Ambily Babu, [11] have described the various source of power dissipation in digital CMOS and the power optimization technique at circuit and device level. And also described the various expression related to power dissipation.

Wasim Maroofi *et al* [10] have described the design methodologies for low power VLSI architecture. In this paper all the methodologies are accomplished in 90nm CMOS technology. And it also describe the importance of extended battery life.

III. POWER DISSIPATION

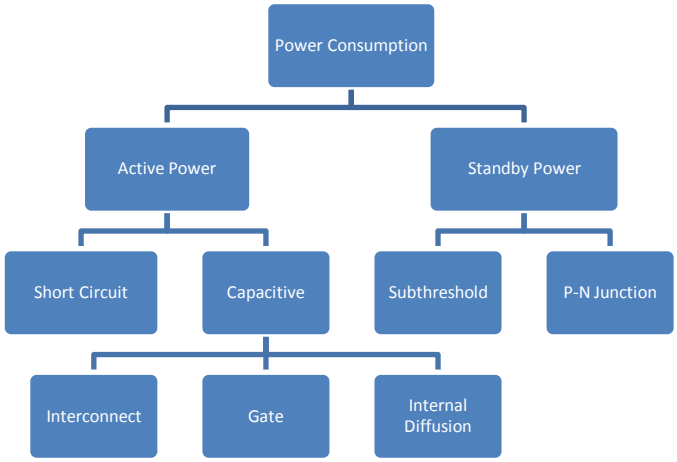
Power dissipation is of basically of two types (1) Static power (2) Dynamic power

Static power is constituted due to leakage currents and it is produced by the reverse bias current whereas dynamic power is constituted by short circuit power and capacitive switching power.

In VLSI clock signal is adopted for the co-occurrence of operational components. Clock power is a crucial component of power predominantly as the clock is delivered to almost all of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a significant component of the overall power dissipation in the digital circuit clock gating technique , clock to an idle portion is disabled, thus refraining power dissipation due to unwanted charging and discharging of the unutilized circuit. In clock gating, clock is stopped for a portion of circuit selectively that is not executing any vital computation .Local clocks which are enabled on the basis of conditions are referred to as gated clocks, as any signal from the environment can be used for gating the global clock signal. Total power dissipated by a digital circuit is given by:

$P_{(Total)} = P_{(Static)} + P_{(Dynamic)} + P_{(Short\ Circuit)}$

P_{total} is the total power dissipation, $P_{dynamic}$ is the dynamic power dissipation due to switching of transistors, $P_{Short\text{-}circuit}$ power is the short-circuit current power dissipation when there is a direct current path from power supply down to ground.



IV. SOURCES OF POWER DISSIPATION

Power consumption in digital circuits can be divided into two categories:

1. Static power
2. Dynamic power

1. Static Power: It is the power exhausted by gate when the gate is idle. Ideally, CMOS (Complementary Metal Oxide Semiconductor) circuits do not exhaust static (DC) power as no direct path from V_{dd} to ground exists in the steady state .

$$P_{Static} = I_{Leakage} . V_{dd}$$

2. Dynamic Power : It is the power exhausted when gate is in active state .It is due to switching activity of input signal. Or we can say that, dynamic power dissipation is originated due to charging.

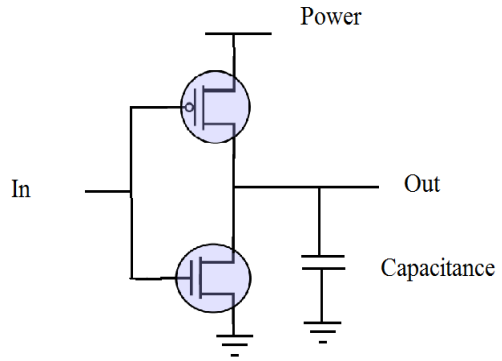
Dynamic Power

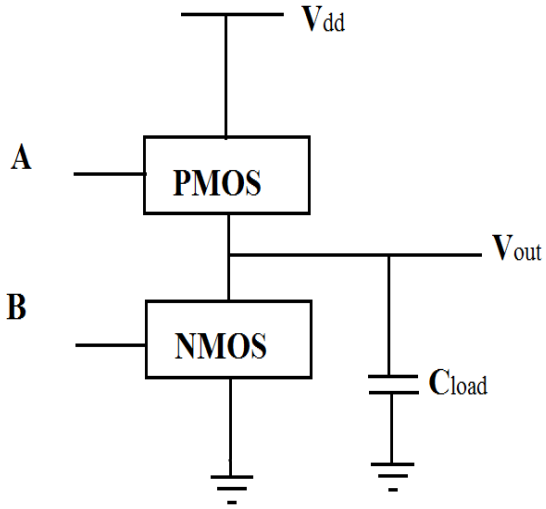
The power which is exhausted by the gate when it is in active state is known as dynamic power. It originates due to switching activity of input signal. There are two components of switching activity: 1.which determines the average periodicity of data arrivals 2 .E(sw) which will determine how many transition each arrival will generate. It is reduced by (i) selecting proper algorithms architecture optimization (ii) proper choice of logic topology

(iii)logic level optimization which results in less power.

$$P_{Dynamic} =\propto C_L V_{DD}^2 F$$

Dynamic power can be reduced by reducing chip area, advanced interconnect , supply voltage scaling, better design techniques, appropriate power management strategies. The various parameters that can be varied are: 1.reducing clock frequency 2. load capacitance 3.Rail voltage 4. switching activity parameter. Reducing clock frequency is the easiest but it also affects the performance of the chip. Reducing load capacitance is another method to reduce the dynamic power. It involves conscientious system design, so that there are fewer wires ,smaller pins, smaller fan_out, smaller devices etc. The rail voltage Vdd can be reduced through the device technology. It is also dependent on the threshold voltage and noise margin. Some specific techniques are also included in reducing power dissipation. The first one is pipelining to operate the internal logic at a lower clock than the input output frequency. Switching activity parameter is reduced by optimizing algorithms, architecture, logic topology , and some special encoding techniques.





C_{load} Depends on : 1.Output node capacitance of the logic gate : due to drain diffusion region. 2. Total interconnect capacitance : has higher effect as technology node shrinks 3.Input node capacitance of the driven gate: due to gate oxide capacitance.

Dynamic Power Dissipation is basically contributed by three types of power dissipations namely :

1. Switched Power Dissipation 2. Short circuit power dissipation 3. Glitch Power Dissipation

Switched Power Dissipation is due to charging and discharging of the load capacitance connected in the circuit.

$$P_{Switc\ hing} = a.C_{Load}.V_{dd}^2.f_{clk}$$

Short Circuit Power Dissipation is due to the DC path that exists between the supply and ground during the output transition. When both NMOS and PMOS may be ON at once Short Circuit path is created and hence short circuit power is dissipated.

$$P_{Short\ Circuit} = I_{SC}.V_{DD} = \frac{\beta}{12}(V_{DD} - 2V_t)^3\ \tau/T$$

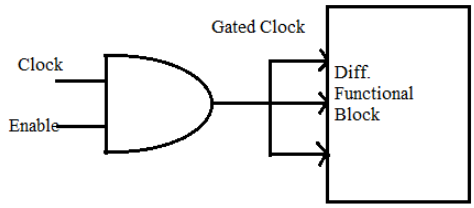
Glitch Power Dissipation is caused due to the skew in the input signal to the gate. Glitches are temporary changes in the value of the output unwanted transitions.

$$P = \frac{1}{2}.C_L.V_{dd}\,(V_{dd} - V_{\min})$$

V. DYNAMIC POWER REDUCTION OF VLSI CIRCUITS BY:

1. Clock Gating Technique

Clock Gating Technique is accepted widely in the industry that disables clock to the idle portions of chip, hence reducing power dissipation because of charging and discharging of the not used circuit.



In clock gating, clock is selectively stopped for idle portions of the circuit by using enable signal.

2. Supply Voltage

As there is quadratic relationship between supply voltage and power, reducing the voltage is most effective method for decreasing the power. But reducing the supply voltage increases the delay in the circuit as supply voltage is reduced to threshold voltage of the device. Solution to this problem is creating the voltage islands. Voltage island is the concept of multiple supply voltages that are being used in different functional blocks of the core for saving the power. The functional blocks are of two types: 1.Critical 2. Non-Critical. High supply voltage is given to critical blocks and low supply voltage is given to non-critical blocks thus creating a perfect balance between performance and power. It can be achieved using level shifters.

3. Load Capacitance

The device capacitance and the interconnect capacitance both effects the parasitic load capacitance. The device capacitance can be decreased by proper transistor sizing. But doing so affects the performance because it decreases the current drive of the circuit. A solution to this problem is to calculate the slack time at each gate connected in the circuit. Slack time is defined as the difference between the signal's required time and the arrival time of the signal at the output of the gate. The size of gate are adjusted as if the slack time is as less as possible.

4. Switching Activity Factor

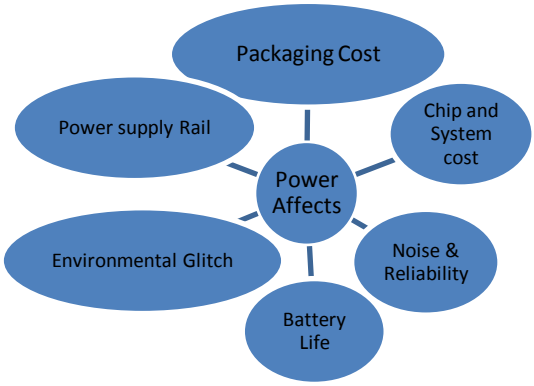
Together with load capacitance and supply voltage, the switching activity factor also influences the dynamic power dissipation of any circuit. A chip can contain a large no of load capacitances, but if there is no switching, no dynamic power is consumed. Static logic family have lower activity factor but dynamic circuits having clocked nodes have higher activity factor.

5. Frequency

Frequency also affects the dynamic power dissipation of the circuit. Higher is the frequency of the circuit higher is its dynamic power dissipation. Therefore to reduce the dynamic power dissipation frequency is to be reduced, wherein the major concern is throughput not the frequency.

VI. WHY LOW POWER?

Low Power is considered because of various factors which are affected due to it:



VII. PERFORMANCE PARAMETERS

A. Supply Volatge:

Their is a quadratic relation between power and voltage, and this relationship offers most effective method for reduction in power dissipation.

We know that :

$$P_{dynamic} = \alpha.C_L.V_{dd}^2.f$$

$$P = V^2 \div R$$

This equation implies that if V is reduced than Power is also reduced.

B. Physical Capacitance:

Dynamic power dissipation depends on switching capacitance of the circuit. Charging and Discharging of load capacitance C_L plays an important role and is given by:

$$P = 0.5CV_{DD}^2.E(sw)f_{clk}$$

Where C is physical capacitance of the circuit
V_{DD} is power supply
f_{clk} is clock frequency
E(sw) is switching activity.

C. Switching Activity Factor:
Switching Activity also influences the Dynamic Power Dissipation of the circuit. As dynamic families have clocked nodes and therefore a high activity factor. For this Clock Gating technique is used to reduce the dynamic power by disabling the clock to idle portions of the circuit.

D. Frequency:
Frequency of the circuit can be reduced to reduce the dynamic power.

VIII. FUTURE SCOPE

Dynamic Power Reduction is a major consideration that needs to be utilized where power conservations is the prime goal. Our future work includes estimation of power for non-monotone transitions and estimating error in short circuit power estimation.

IX. CONCLUSION

In this paper , various power reduction techniques are reviewed. Design for low power CMOS circuits implies the skill to reduce the power consumption. Various technologies have various tradeoffs and their selection is made as per the requirement. It can help the designers to understand the basics of low power. The main issues were reviewed and explained. Future challenge in this field is to make a perfect balance between various factors that contribute to dynamic power dissipation.

REFERENCES

[1]. Sung-Mo Kang, Yusuf Leblebigi "CMOS Digital Integrated Circuits Analysis and Design" , McGraw-Hill Higher Education, 3rd edition 2003.

[2]. Gary K. Yeap, "Practical Low Power Digital VLSI Design" , Kluwer Academic, Publishers, 1998.

[3]. Mr. Suhas D. Kakde, Mr. P. B. Pokle, Mr. Jayantkumar Dorave "Low Power VLSI Design Methodologies & Power Management" in *ijrat*, Vol.4, No.4, April 2016.

[4]. Kanika Kaur and Arti Noor, "Strategies & methodologies for low power vlsi designs: a review",International Journal of Advances in Engineering & Technology, May 2011. ISSN:2231-1963.

[5]. Massoud Pedram "Design Technology for Low Power VLSI" in *ijrat*, 1995.

[6]. www.wikipedia.com on Nov 10 2017.

[7]. Luca Benini & Giovanni De Micheli, "Dynamic Power Management, Design Technique and CAD Tools", Kluwer Academic Publishers, 1998.

[8]. Abdellatif Bellaouar & Mohamed I. Elmasry, "Low-Power Digital VLSI Design,Circuits and Systems", Kluwer Academic Publishers, 1995.

[9]. Kamal K Mehta, "A Review on Strategies and Methodologies of Dynamic Power Reduction on Low Power System Design" *in ijcsc* Volume 7, No 1, 2016.

[10]. Wasim Maroofi, Sanjay R. Ganar, "Review on Design Methodology for Low Power VLSI Architecture" *in ijarcce*, Volume 5, Issue 6, June 2016.

[11]. Ambily Babu, "Power Optimization Technique at circuit and Device Level in Digital CMOS VLSI- A Review" in *ijert* volume 3 , Issue 11, November 2014

[12]. P.R. et al., "Power-efficient System Design" , DOI 10.1007/978-1-4419-6388-8_2, © Springer Science + Business Media, LLC 2010

[13]. A.P. Chandrakasan and R.W. Broderson, "Minimizing Power Consumption in Digital CMOS Circuits," Proc. of the IEEE, vol. 83, pp. 498-523, April 1995.

[14]. A.P. Chandrakasan, "Low Power CMOS Digital Design, " IEEE J. Solid State Circuits vol. 27 no 4 pp. 473-478, 1992.

[15]. D. Liu and C. Svensson, "Power Consumption Estimation in CMOS VLSI Chips, " IEEE Journal of Solid-State Circuits, vol. 29, pp. 663-670, June 1994.