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Performance Analysis of Frequency and Tuning Range of Ring Oscillator: A Review

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***Abstract*— This paper presents a review of CMOS inverter and its mathematical modelling for determining aspect ratio. Ring oscillator is a cascading of odd number of delay cell. Power consumption, phase noise, figure of merit and tuning range are important parameter used in designing of ring oscillator. There is trade-off between phase noise and power consumption. A concise attempt has been made to discuss various topology used in designing of ring oscillator in order to improve the frequency range and reduce chip area with minimum power.**

Index Terms— **Ring Oscillator (RO), Inverter (delay stage), Voltage Control Oscillator (VCO), Tank Circuit (LC).**

I. INTRODUCTION

Ring oscillator (RO) is widely used in analog and digital circuits. It is used as voltage control oscillator (VCO) in clock recovery circuits. VCO is most important blocks in radio frequency communication systems, musical instrument etc. In electronic system, oscillator is key element in designing of Phase Locked Loop (PLL), Digital PLL (DPLL), Cyclotrons, Frequency synthesizer and telecommunication systems.

In oscillator designing LC tank circuit is used for providing better frequency performance and phase noise improvement. But implementation of inductor is very difficult and limited by parasitic effect. LC tank circuit provides tuning range/channel selection.

VCO is a part of electronic circuit which converts the input voltage into its corresponding frequency at the output. VCO is mostly used in PLL, DPLL. Oscillator has maximum tuning range, phase noise, and frequency. Operating frequency and delay time is important in feedback path. RO is designed with different CMOS process technology and provide result in different interest of area that is it provides stability increment decrement, frequency range variation power optimization, tuning range variation.

RO consist of an odd number of inverters or delay stages [2]. Oscillations are varied using addition of inverter stages and the same provides the frequency range. Addition of more inverting stages increases propagation delay of the circuit.

Propagation delay is related to the number of stages which adds frequency of oscillation. It is not practically acceptable when addition of inverting stages goes beyond nine. It increases dissipating power of the circuit. Power is important parameter in VLSI designing. Conventional CMOS RO produce high frequency signals but when large number of delay cells are added, they produces low frequency and consumes more power. It gives very low oscillating frequency when hundreds of an inverting stage added but it is difficult to design and fabricate [7]. Range of frequency variation is several MHz to GHz in VCO. LC VCO is used to achieve lager range of frequency of oscillation but face some problem like fabrication complexity, high power consumption and large phase noise. A good VCO design must satisfy ideal characteristics which includes minimum phase noise, lower power consumption, high gain factor and high frequency linearity.

This paper presents basic of RO and its design, type of VCO and comparison of result. This Paper consolidated as follows:

Section II Describes CMOS inverter
Section III Discusses about voltage control oscillator
Section IV Describes applications of VCO
Section V Includes comparative analysis of published result
Section VI Presents conclusion.

II. CMOS INVERTER

CMOS inverter is a concatenation of p-type and n-type transistor. It important and basic block of CMOS oscillator. Inverter performs logical inversion operation of input. PMOS is connected with V_{dd} supply and NMOS connected to V_{ss}. When the input is high PMOS is OFF, NMOS is ON state and the output voltage is pull down to ground. When the input is low NMOS is OFF, PMOS is ON and the output is pulled up to supply. Schematic of CMOS inverter is shown in Fig1.

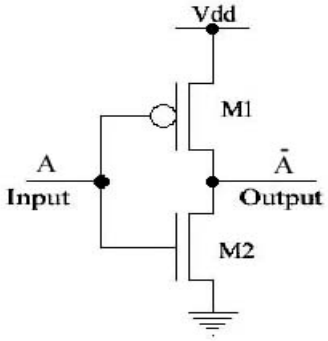

Fig1: schematic of CMOS inverter

Input A=High; M2=ON, M1=OFF; Output=Low
Input A=Low; M2=OFF, M1=ON; Output=High

W/L Ratio (Aspect Ratio) for MOS Transistor

The threshold voltage V_{th} of MOS transistor is an important to characterized steady state characteristic of an inverter stage used in designing of PMOS and NMOS devices.

W= width of transistor, L= length of transistor

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$$\sqrt{\frac{1}{K_r}} = \frac{V_{th}-V_{ton}}{V_{dd}-V_{th}+V_{top}}$$

K_r= Transcondutance parameter ratio and is given as,

$$K_r = \frac{K_n}{K_p}$$

Where,
K_n = device transconductance of NMOS transistor
K_p = device transconductance of PMOS transistor
V_{th}= threshold voltage
V_{ton}= threshold voltage (n-channel transistor)
V_{top}= threshold voltage (p-channel transistor)
V_{dd}= supply voltage
Simplifies and get K_r

$$K_r = \frac{K_n}{K_p} = \frac{(V_{dd}-V_{th}+V_{top})^2}{(V_{th}-V_{ton})^2}$$

V_{th} for an ideal inverter is

$$V_{th\ ideal} = \frac{1}{2}V_{dd}$$

Now solving K_r with $V_{th\ ideal}$ and we get result as

$$\left(\frac{K_n}{K_p}\right)_{ideal} = \frac{(0.5V_{dd}+V_{top})^2}{(V_{dd}-V_{top})^2}$$

Devices PMOS, NMOS operation are complemented to each other in CMOS inverter, Hence
$\left(\frac{K_n}{K_p}\right)_{symmetric\ inverter}$ =1
Hence K_r as,

$$\frac{K_n}{K_p} = \frac{\mu_n C_{ox(W/L)_n}}{\mu_p C_{ox(W/L)_p}}$$

C_{ox} = oxide capacitance
μ_n= electron mobility
μ_p= hole mobility

Assuming C_{ox} is equal for both MOS devices then

$$\left(\frac{W}{L}\right)_p = 2.5\left(\frac{W}{L}\right)_n$$

Thus W/L ratio of PMOS is 2.5 times that of NMOS

III. VOLTAGE CONTOL OSCILLATOR

VCO is important block in radio frequency wireless communication system. It converts input voltage into output frequency. There are two types of VCO as Waveform oscillator and resonant oscillator.VCO having good control and hold range. VCO provides clock circuitry for design. It adjusts frequency with PLL and filter and similar to RO whose frequency of oscillation controlled by current with the help of inverter.

Basic principle for an oscillation is that it must satisfy Barkhausen criteria that is loop gain (A) is unity and phase shift (PS) should be 360degree or zero degree.
A=1
PS=$0^0/360^0$
Basic block diagram of VCO shown in fig2 [4]

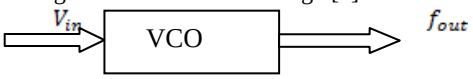

Fig2: Block diagram of VCO

VCO act as a converter which convert the input voltage to its correspond frequency output. VCO is classified into two categories as –

- WAVEFORM OSCILLATOR
  A) RO topology
  B) Relaxation oscillator

- RESONANT OSCILLATOR
  A) LC tank oscillator
  B) Crystal oscillator

In this paper we have discussed the design aspects of ring oscillator.

A. *RING OSCILLATOR*

RO is sequential connection of inverter with feedback path. Output of last stage of delay is feedback to the first stage of inverter as input of the circuit. It is used in on-chip clock distribution, frequency synthesizers etc.
If less number of delay stages are used in designing of RO, it will result in higher frequency of oscillation and less power consumption. Applied voltage beyond permissible range of RO, limit its . speed. Various topologies are used in designing of RO to get low frequency range, save power and small chip area. CMOS thyristor technique is used to produce low frequency and consume low power [8]. A five inverting stages/delay cell Simple RO in shown in Fig3. In this all delay cell connected to each other

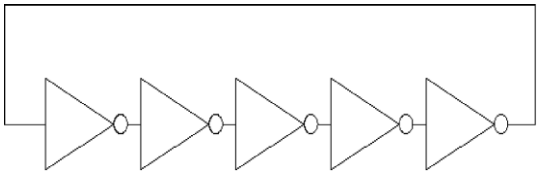

Fig3: Schematic of RO with 5 stages [1]

In RO propagation delay and number of stages is most important parameter to calculate frequency of oscillation. Propagation delay occurs due to transition of state of each stages that is high-to-low and low-to-high. Schematic of conventional RO with three stage shown in Fig4.

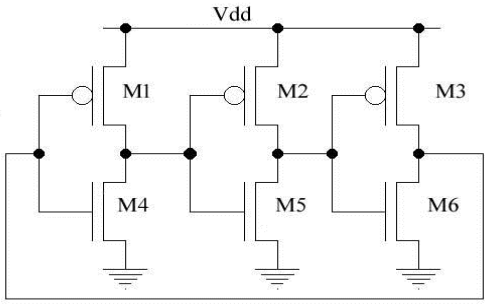

Fig4: Conventional RO [1]

Mathematical equation that provide oscillation frequency of output waveform is given by

$f_o = \frac{1}{2NT_d}$

f_o = oscillation frequency

N = number of inverting stages

T_d =propagation delay occurring due to transition of level [8].

$T_d = \frac{T_{PHL}+T_{PLH}}{2}$

T_{PHL} = propagation delay when state transition from high-to-low

T_{PLH} = propagation delay when state transition from low-to-high

B. VCO Specifications are

Tuning range

Tuning range of VCO is linear with control voltage and output frequency [12].

$$f_{out}=f_o+K_{vco}*V_{control}$$

f_{out}= Output frequency

f_o= Oscillation frequency

K_{vco}= Sensitivity

V_{con}= control voltage

Definition of K_{vco} shown in figure 5:

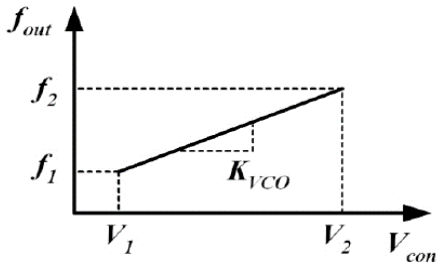

Fig 5: definition of K_{vco} [12]

Phase noise

Phase noise is signalized in frequency domain of signal. Some unwanted signal skirts exhibits around the centre frequency.

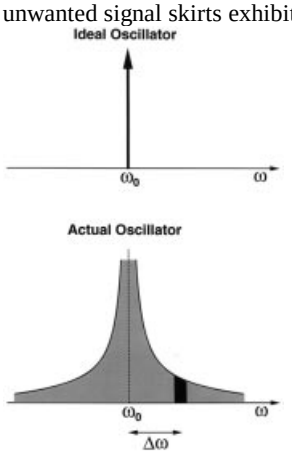

Fig 6: Spectrum of an oscillator

Power consumption

Power consumption is directly calculated by the total current (I_{total}) and equivalent resistance (R_{eq}) [12]. Power and phase noise of oscillator should be low but it is difficult to maintain low phase noise and low power consumption simultaneously.

$$V \approx I_{total}.R_{eq}$$

Figure of merit (FOM)

It is a quantity used to signalize the performance of device/system.

Figure-of-Merit (FOM) of oscillator can be expressed as

$$FOM=L(\Delta\omega) - 20\log\left[\left(\frac{w_o}{\Delta\omega}\right)\right] + 10\log\left(\frac{P_{diss}}{1mW}\right)$$

Where, w_o is oscillator frequency, $P_{diss}$is power dissipation (mw), L(Δω) is phase noise spectral density, Δω is centre frequency .

IV. APPLICATIONS

RO is used in telecommunication system, measuring the effects of temperature & voltage on chip. It is used to design PLL. Many wafers have a RO which act as scribed line test structures. They are used for measuring the effects of manufacturing process variation during wafer testing. Jitter of RO is used in hardware random number generator.

V. COMPARATIVE ANALYSIS OF PERFORMANCE METRICS (PUBLISHED RESULT)

References	[1]	[2]	[3]	[5]	[6]
Types	RO	RO	RO	RO	RO
Process technology(nm)	350	180	50	180	90
No of stages	3	5	5	7	2
Operating Voltage(v)	3.5	1.8	1	1.8	1.5
Power consumption(mW)	6.22	0.054	0.064	5.2	9.6
Tuning range(%)	80	81	72	12	62
Frequency range(GHz)	--	1-3.12	0.7-2.56	1.5-3	1.2-3.2
Phase noise(dBc/Hz)	--	--	--	-94.8	-90.01

This table contains comparative analysis of VCO specification based on published result. There is a tabular comparison between Phase noise, frequency range, tuning range, operating voltage,

power, number of stages used, and process technology with references.

VI. CONCLUSION

In this paper conventional RO with its different blocks, mathematical modelling and features has been discussed. According to the published results chip area, power consumption and frequency range are important parameters for designing of RO. Low frequency range conventional RO contains large number inverter stage which consume more power and lager chip area. Various topologies used to design RO to improve frequency range, save power and small chip area has been analyzed in this paper.

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