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An Experimental Analysis of Seventeen Level Three Phase Cascaded H-Bridge Multilevel Inverter Topology

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Abstract: The research on cascade H-Bridge multilevel inverter topology,in these days for various applications goes on increasing rapidly due to its systematic operation. This paper proposes the experimental analysis of 17- level inverter topology with 3-phase induction motor load. The simulation results ofoutput voltage wave forms are experimentally verified.

Key words: Induction motor, inverter, voltage, Dc Source. Equal area criteria.

INTRODUCTION

Number of industrial applications have initiated using high power conversion system in present days. Nearly low and medium voltage motor drives are used for industrial applications and ability in applications require low, medium voltage and high power level for a medium voltage grid; it is worrying to connect directly a single switch. As a result, multilevel power converter has been introduced as an alternative in high power and medium voltage situations.

The multilevel inverters has been introduced later 1975. The term multilevel starts with the three level inverters. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms with less harmonic content, less switching frequency, higher efficiency, lower voltage stress on the devices and better electro-magnetic compatibility. A multilevel inverter have high power ratings, as they can be used for of renewable energy sources. Renewable energy sources such as photo voltaic, wind and fuel cells can be easily interfaced to a multilevel inverter (converter) system for a high power application. The multilevel power converters can also be known as voltage synthesizers in which high output voltage is synthesized from many smaller voltages levels.

The advantage of multilevel converters when compared to other converters can be listed as follows: they can generate output voltages with extremely low distortion and lower (dv/dt), they draw input current with very low distortion, they can operate with a lower switching frequency, their efficiency is high (>98%) because of the minimum switching frequency, they are suitable for medium to high power applications, multilevel waveform naturally limits the problem of large voltage transients. The selection of the best multilevel topology for each application is often not clear and is subject to various engineering trade-offs. The different multilevel

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topologies are, Diode-clamped multilevel inverter, Capacitor-clamped multilevel inverter and Cascaded multilevel inverter.

Types OF MULTILEVEL INVERTER

1. Diode Clamped or Neutral Point Clamped(NPC) Multilevel Inverter

The first practical multilevel inverter topology is the Neutral Point Clamped PWM technology first introduced by Nabeetal in1980. For mlevel inverter, dc bus voltage is splits into 'm' levels by (m-1) series connected bulk capacitors. Here, diodes clamp the switch voltage to half the level of the dc bus voltage, which is an added advantage of this type. This multilevel inverter has some disadvantages than the cascade multilevel inverter. But it has some advantages as follows. This multilevel inverter is difficult compare to the cascade multilevel inverter. Excessive clamping diodes are required when levels are high. The issue of maintaining the charge balance of the capacitors is still an open issue for NPC topologies with more than three levels.

2. Flying Capacitor Multilevel Inverter

This topology was first proposed in 1992 and is considered to be the serious alternative to the diode clamped topology. In addition to improving the waveform quality, these multilevel inverters substantially reduce voltage stress on the devices. However in this type of inverters required voltage blocking capabilities of the clamping diodes at higher levels is high. So an alternative multilevel structure where the voltage across an open switch is constrained by clamping diodes has been proposed by Maynard. These inverters are commonly known as flying capacitor multilevel inverters. This makes the topology attractive even for the dc/dc conversion. At the present time it seems that this topology has few advantages like: Large amount of storage capacitors can provide capabilities during power outages, like diode clamped inverters, when the number of levels is high enough, the harmonic content is low enough to avoid the need for filters, and both real and reactive power flow can be controlled. Some of the disadvantages of flying capacitor topology are: Excessive number of storage capacitors is required, the inverter control can be very complicated.

3.Cascaded Multilevel Inverter

This topology employs a cascade of low voltage H-bridges each with independent and isolate DC sources. The phase output voltage is synthesized by the sum of series of Hbridges plus one. This cascade multi-level inverter has more capacity compare to other multilevel inverter topologies. One major advantage of this approach is that the number of the output can be further increased without addition of any new components, requiring only the dc sources with different voltage levels.The number of possible output voltage levels is more than twice the number of dc sources (m =2s+ 1).

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The series of H-bridges makes for modularized layout andpackaging,this will enable the manufacturing process to be done more quickly and cheaply. Separate dc sources are required for each of the H-bridges.

Modulation Technique

Equal Area Criteria (EAC):

This method tries to solve the harmonics elimination problems from a totally different angle of approach, no need for high-order multi-variable polynomial equations would be solved in this method.

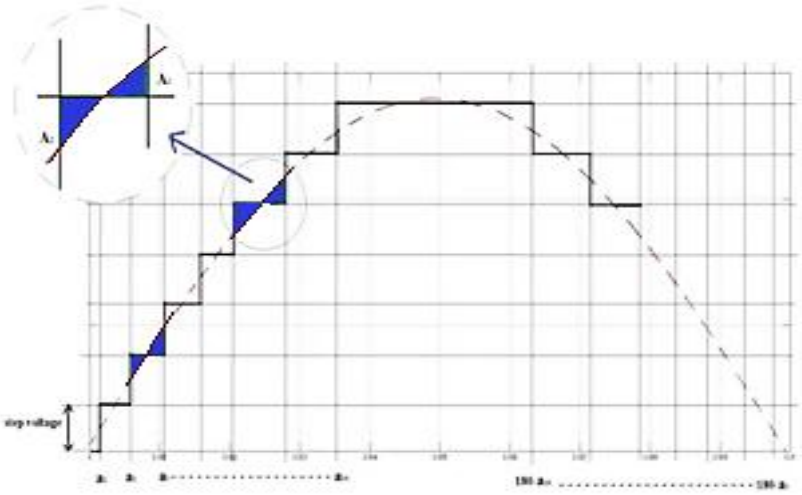

Fig. 1 Equal Area Criteria (EAC) switching technique

In this method we can calculate the best switching angles by dividing half of fundamental sine wave horizontally and vertically with step voltage and time in (m-s) respectively. If the horizontal and vertical lines drawn in such way that the areas $A_1$and A_2 are equal to get minimum total harmonic dissertation (THD). The fundamental switching frequency is taken as 50Hz, the step voltage is a minimum voltage that connected in level generation cell (LGC) in the topology. If the a_1, a_2, a_3, a_n are the switching angles for N-level inverter topology then the angles should be less than 90^0.

$0<a1<a2<a3<a4<a5<a6<a7$ - - - - $an<90^0$

Number of switching angles for N-levels = [(Number of levels-1)/2]

Mathematical formula for angle calculation:

N^{th} switching angle in (deg.) = [[Time at which the N^{th} level vertical line touches the time axis (x-axis)]*[2*fundamental frequency]]*180^0.

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Using this mathematical formula for N-number of levels the switching angles can be calculate.

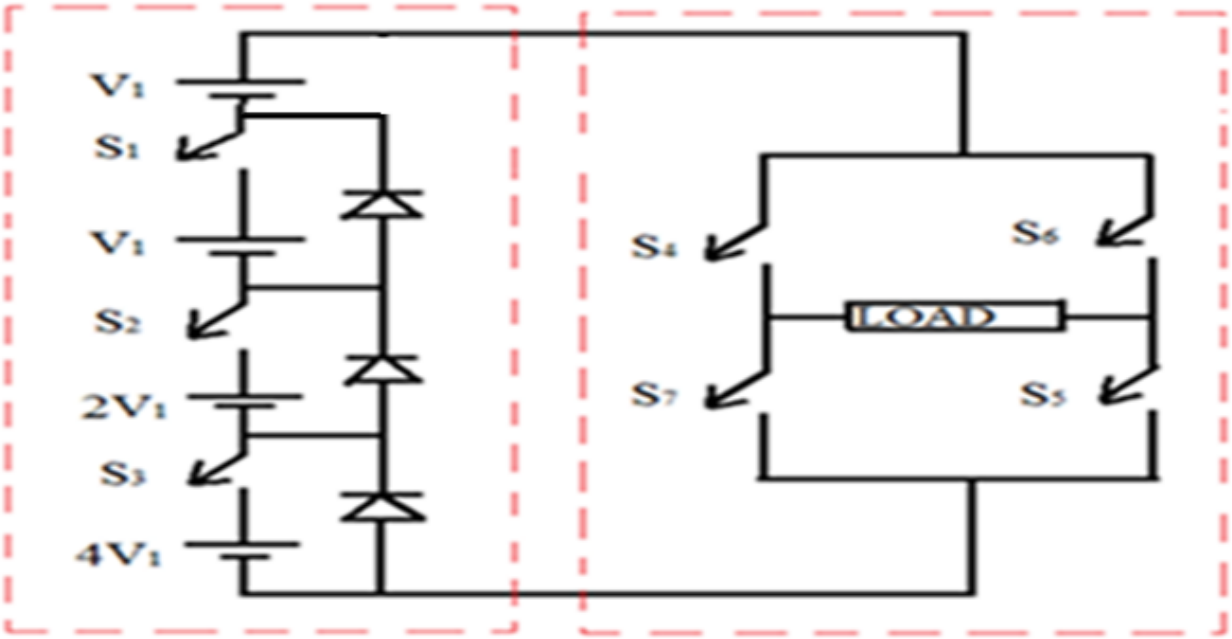

Figure 2: New simplified 17-level multilevel inverter topology

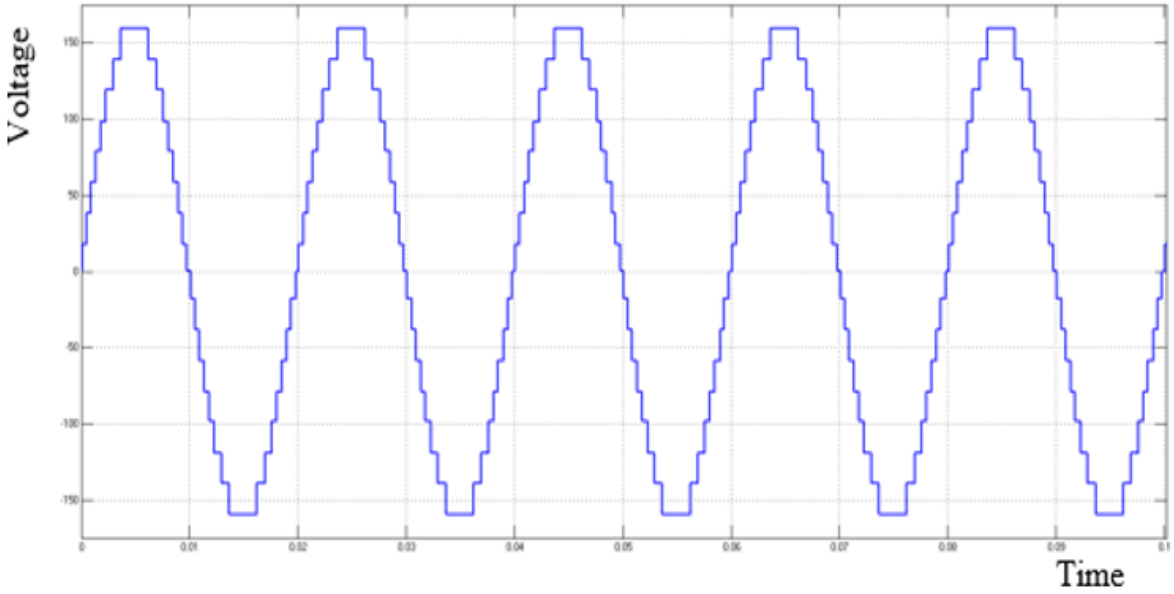

Figure 3: Output voltage waveform of 17-level (y-axis=20V/div. x-axis=10ms/div.)

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Simulation results of Three Phase 17-Level Inverter Topology

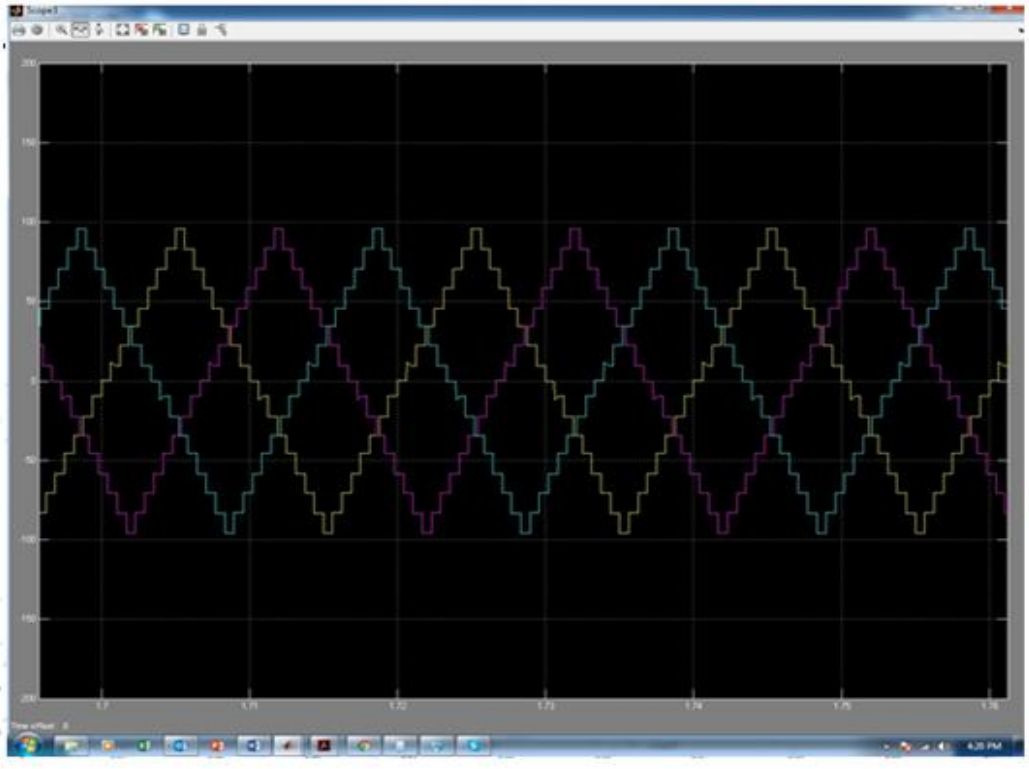

Figure 4: 3-phase 17-level inverter output phase voltage waveforms with R load

Simulation output phase voltage waveforms with resistive load of 3-phase 17-level inverter has shown in fig. 4, with phase shift of 120^0 each other.

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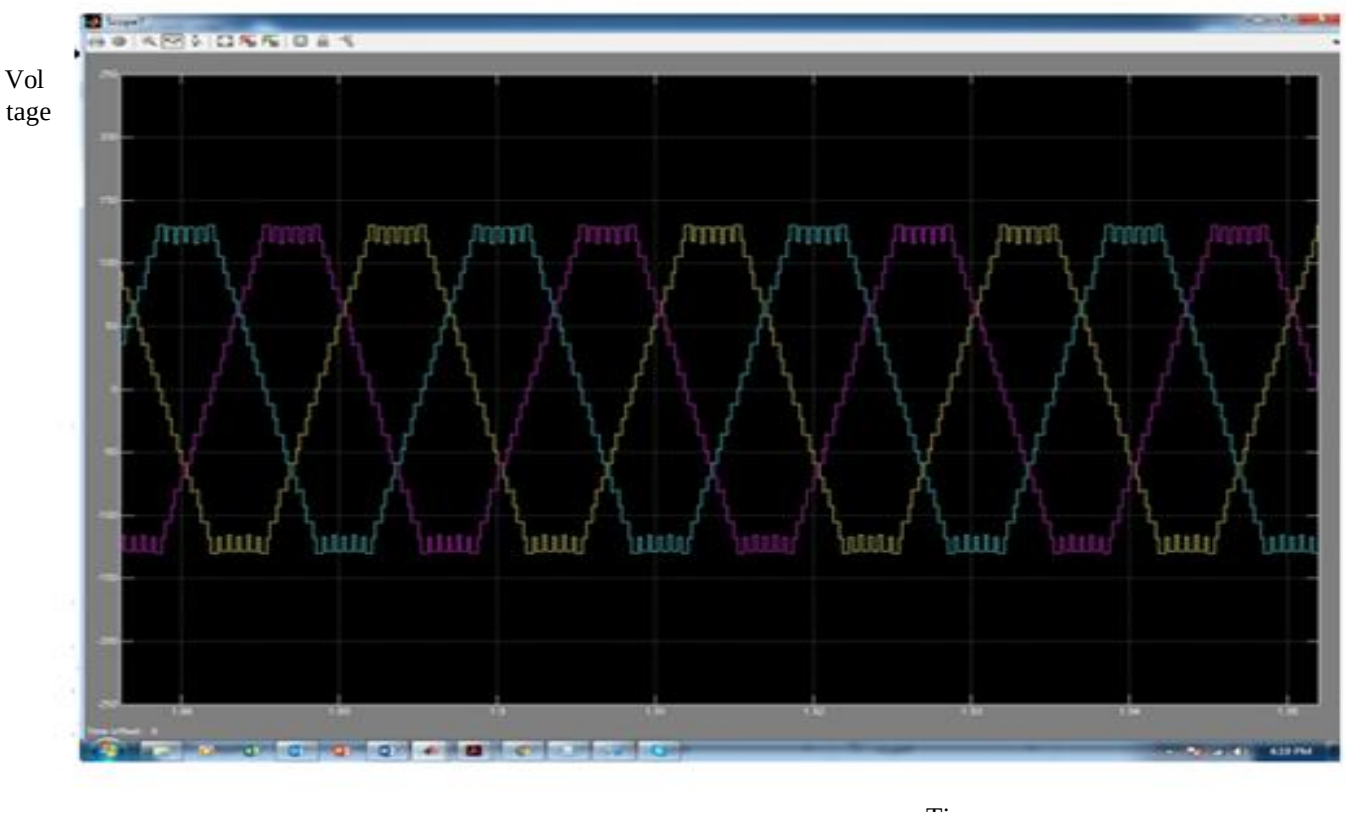

Figure 5: 3-phase 17-level line voltage waveforms with Resistive load.

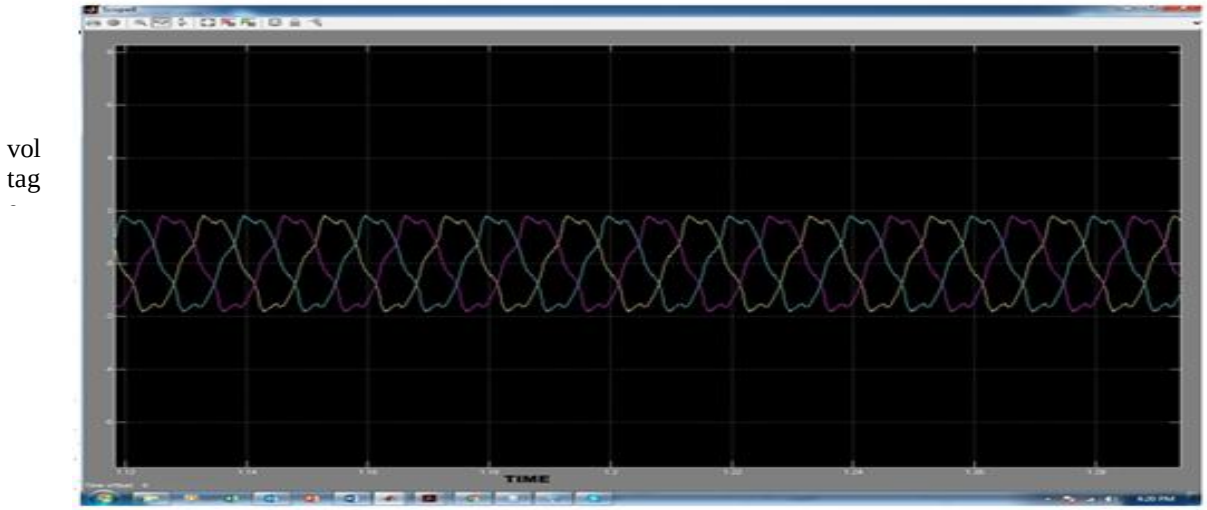

Figure6: 3-phase 17-level current waveforms with Resistive load.

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Experimental analysis of proposed 17 level inverter topology

The hardware prototype model of 17-level inverter block diagram is shown in fig 7.

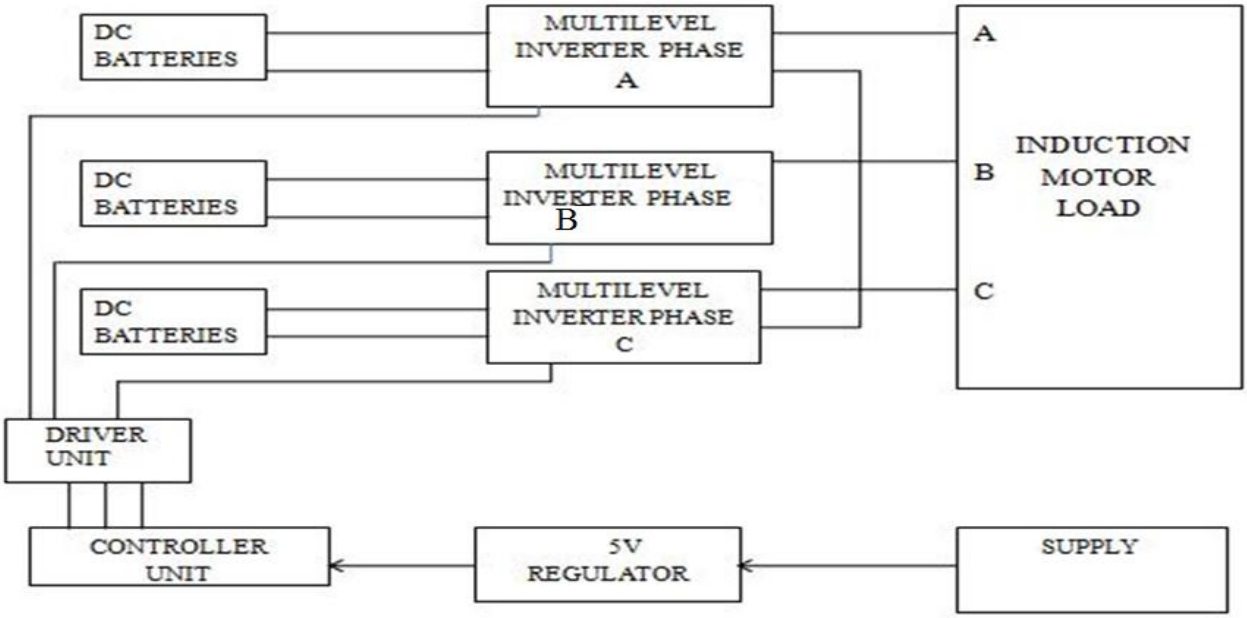

Fig 7: Block diagram of proposed 17-level inverter topology

The 17- level inverter topology each phase of three phase system contains 8 batteries each of 12 volts capacity, so for a 3 phase system 24 batteries are required, in each phase batteries are connected in cascade and which are rechargeable. The output voltage of this batteries is connected to inverter modules for converting DC to AC,the alternating output voltage fed to the 3-phase induction motor.

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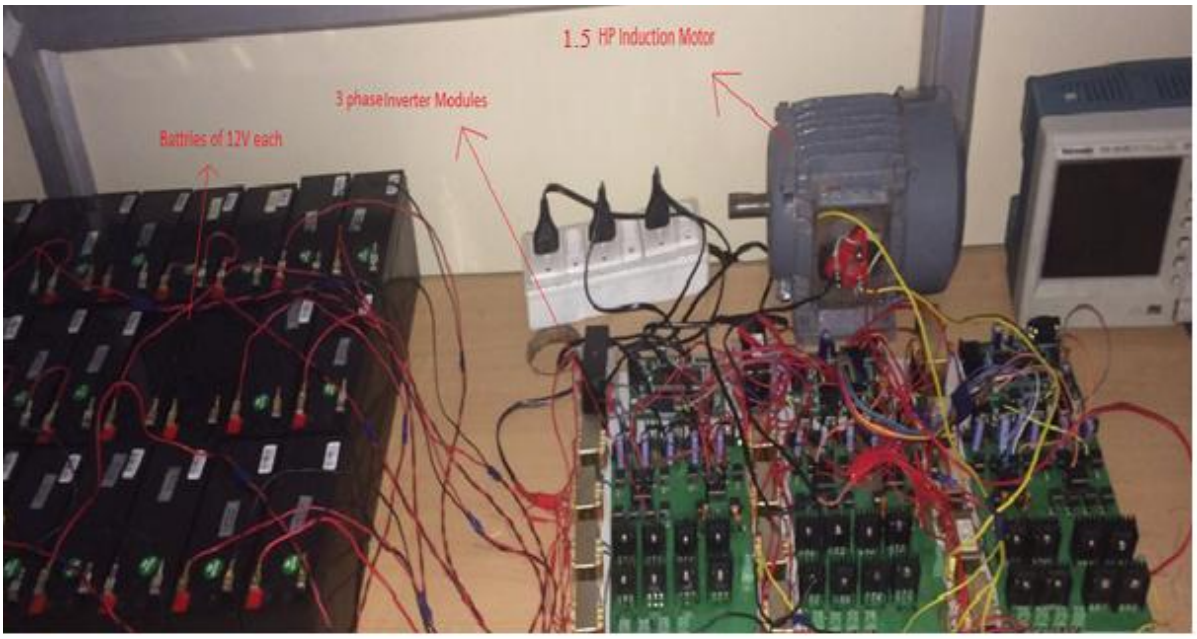

Figure 8: Experimental setup of 17 level multi-level inverter connected to three phase 1.5 HP induction motor with waveforms

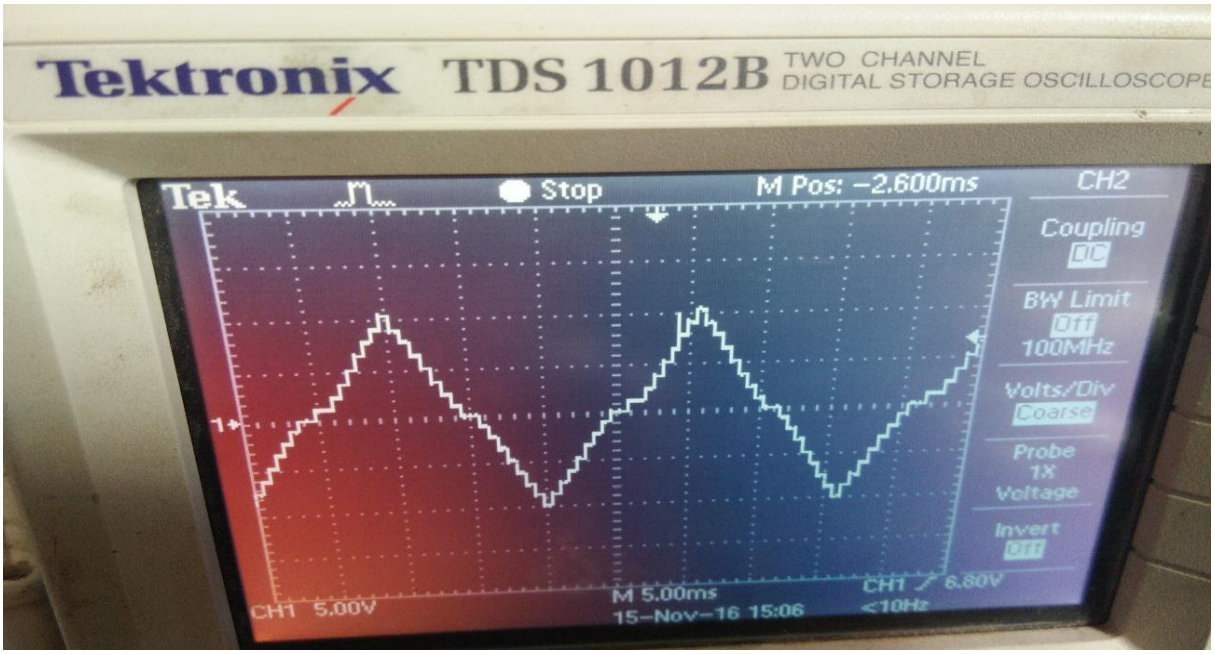

Figure9: Voltage wave form of Single-phase 17 level inverter

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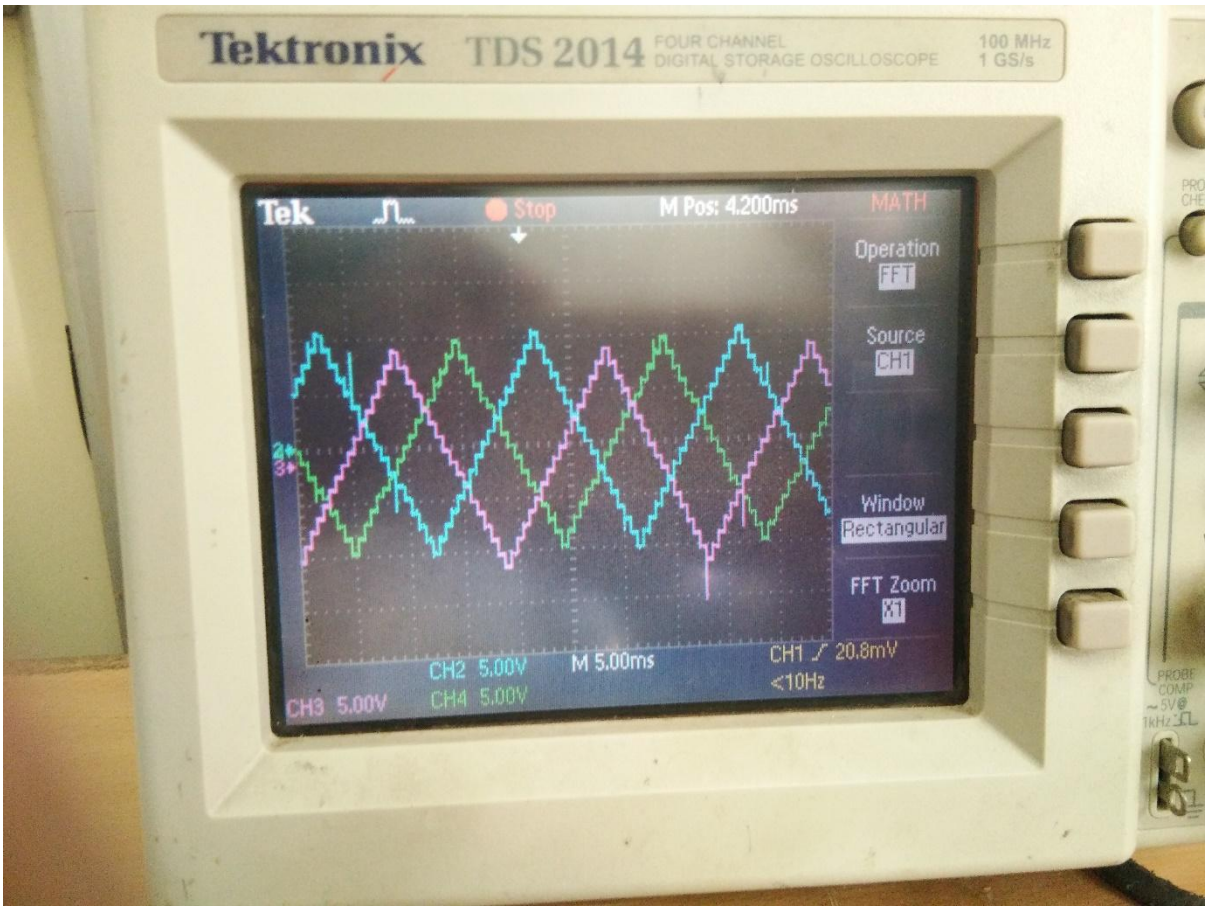

Figure10:Experimental voltagewave forms of 3-phase 17 level multi-level inverter topology

The multilevel H-bridge cascade system model implemented was tested both using simulation and hardware. The simulation was carried using MATLAB simulink. The hardware implementation was carried using various components such as the Power supply, Driver circuits and Microcontroller Unit

Induction motor details:
Ratings:
1.5Hp, 1.2 amps, 220 volts star, 440 volts delta, 3-phase, 50 Hz. 1440 rpm

Parameters:
Inductance /phase = 0.25 henry, inductive Reactance/phase=78.57 ohms,
Impedance/phase =93.07 ohms, resistance /phase = 50 ohms
Output voltages:
Line to line voltage is 87.5volts.
Phase voltage is 71 volts
Load current 0.5A

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CONCLUSION

This paper gives clear idea about the simulation results andare verified experimentally of 3-phase 17-level inverter topology forresistive load and induction motor is successfully driven. As this topology requires less number of switches.

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