ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 7, Issue 4, April 2018

Harmonic Analysis of Different Multilevel Inverters with Inductive Load

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Abstract: Multilevel inverters are power converter system composed by an array of power semiconductor devices which when properly connected and controlled, generates a multistep voltage waveform with variable and controllable frequency, phase and amplitude. Multilevel inverters have brought a tremendous revolution in high power industrial drive applications. Reduction in the harmonic content of the output voltage of a multilevel inverter is a challenging task when the load is inductive (R-L). This paper presents the analysis of 7, 9 and 17 level multilevel inverters topologies with inductive load (R-L) and simulated using MATLAB Simulink then the results are presented. The test results verify the effectiveness of the proposed strategyusing equal area criteria (EAC) as modulation technique to reduce the harmonic content in output voltage of multilevel inverter.

Keywords - Multilevel Inverter; High power applications; Equal area criteria; inductive load; THD;

INTRODUCTION

Power Electronic Converters, are used for conversion from DC to AC power, especially DC/AC PWM inverters have been extending their range of use in industrial applications because they consumed less energy and better system efficiency, converter not only achieves high power ratings but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.The various multilevel topologies, are: Diode-Clamped Multilevel Converter (DCMC) or Neutral Point Clamped (NPC), Flying Capacitors Multilevel converters (FCMC) and Cascaded Multilevel Converters (CMC).

The simplest and the most modular type topology isCascaded Multilevel Convertersas it has not required clamping diodes and flying capacitors. However, the main problem associated with the CMC topology is the need for isolated DC sources which are not usually available without the use of transformers. In some specific applications such as photovoltaic systems, separate DC sources exist and can be used in the CMC topology.

The applications of multilevel converters are in traction, both in locomotives and trackside static converters, now days used in power system converters for VAR compensation, stability improvements and High-voltage DC transmission.

MODIFIED HYBRID MULTILEVEL INVERTER TOPOLOGY

The Modified hybrid multilevel inverter topology consists of two cells one is level generating cell (LGC) and other is polarity generating cell (PGC), the LGC is contains voltage sources and PGC is bridge which is used for changing the polarity of output voltage. In this topology a minimum voltage is connected in LGC is known as step voltage (minimum),for 7-level topology uses the asymmetrical voltages in ratio V1:2V1 with 6 switching devices. This topology requires less number of voltage sources as compared to conventional topology, the topology structure shown in fig 1 and the detailed switching operation of the topology is shown in the table1.

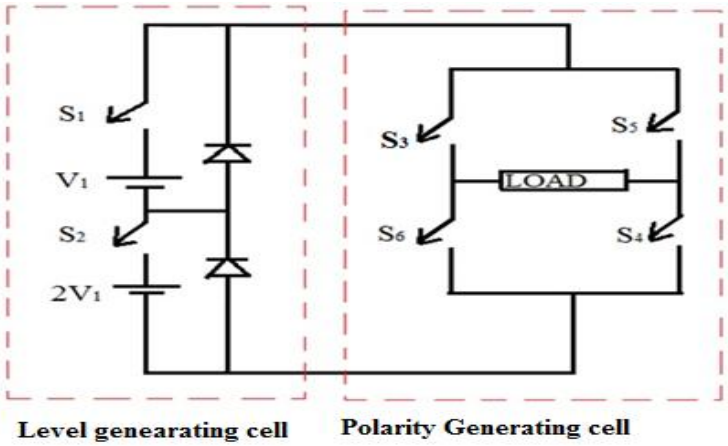

Figure 1. Asymmetrical 7-level Multi-level inverter topology

Sl NO	S1	S2	S3	S4	S5	S6	Output voltage
1	1	0	1	1	0	0	V1
2	0	1	1	1	0	0	2V1
3	1	1	1	1	0	0	3V1
4	0	0	0	0	0	0	0
5	1	0	0	0	1	1	-V1
6	0	1	0	0	1	1	-2V1
7	1	1	0	0	1	1	-3V1

Table 1: Switching sequence of 7-level asymmetrical inverter topology

The simplified 9-level multilevel inverter topology can be obtained through the simple modification of asymmetrical 7-level inverter topology by connecting a step-voltage (minimal voltage). Here V1 is the minimum voltage and asymmetrical voltage source are in the ratio V1:V1: 2V1 here there are 2-cells (LGC) which produces the output levels and

(PGC) is used changes the polarity of the output voltage.The circuit diagram shown in fig 2and detailed switching operation shown in table 2.

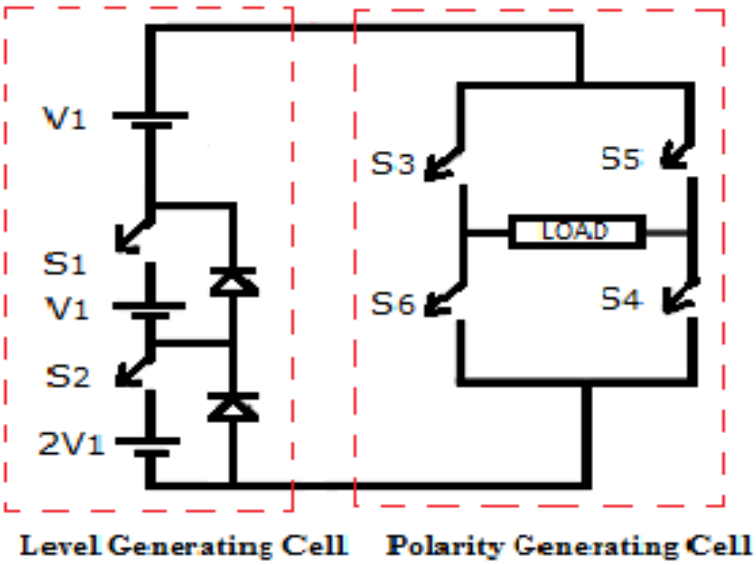

Fig. 2: Asymmetrical9-level multi-level inverter topology

Sl. NO	S_1	S_2	S_3	S_4	S_5	S_6	Output voltage	Number of switching's
1	1	1	1	1	0	0	$4V_1$	2
2	0	1	1	1	0	0	$3V_1$	1
3	1	0	1	1	0	0	$2V_1$	2
4	0	0	1	1	0	0	$1V_1$	1
5	0	0	0	0	0	0	$0V_1$	2
6	0	0	0	0	1	1	$-1V_1$	2
7	1	0	0	0	1	1	$-2V_1$	1
8	0	1	0	0	1	1	$-3V_1$	2
9	1	1	1	0	0	1	$-4V_1$	3

Table 2: Switching sequence of 9-level inverter topology

The new simplified 17-level multilevel inverter topology shown fig.3 can be develop with simple modification of 9-level inverter topology by connecting voltage source 4V1. Here the V1voltage is minimal voltage (step voltage) and asymmetrical voltage source are in the ratio V1:V1:2V1:4V1.The detailed switching operation is shown in table 3.

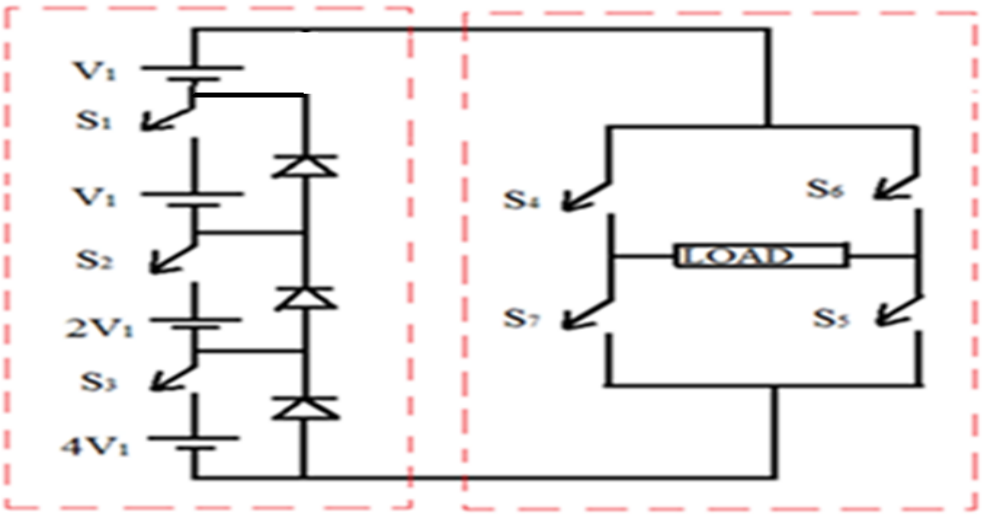

Fig. 3: Asymmetrical 17-level multi-level inverter topology

S.NO	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Output voltage	Number of switching's
1	1	1	1	1	1	0	0	$8V_1$	4
2	0	1	1	1	1	0	0	$7V_1$	1
3	1	0	1	1	1	0	0	$6V_1$	2
4	0	0	1	1	1	0	0	$5V_1$	1
5	1	1	0	1	1	0	0	$4V_1$	3
6	0	1	0	1	1	0	0	$3V_1$	1
7	1	0	0	1	1	0	0	$2V_1$	2
8	0	0	0	1	1	0	0	$1V_1$	1
9	0	0	0	0	0	0	0	$0V_1$	2
10	0	0	0	0	0	1	1	$-1V_1$	2
11	1	0	0	0	0	1	1	$-2V_1$	1
12	0	1	0	0	0	1	1	$-3V_1$	2
13	1	1	0	0	0	1	1	$-4V_1$	1
14	0	0	1	0	0	1	1	$-5V_1$	3
15	1	0	1	0	0	1	1	$-6V_1$	3
16	0	1	1	0	0	1	1	$-7V_1$	2
17	1	1	1	0	0	1	1	$-8V_1$	1

Table 3: Switching sequence of 17-level inverter topology

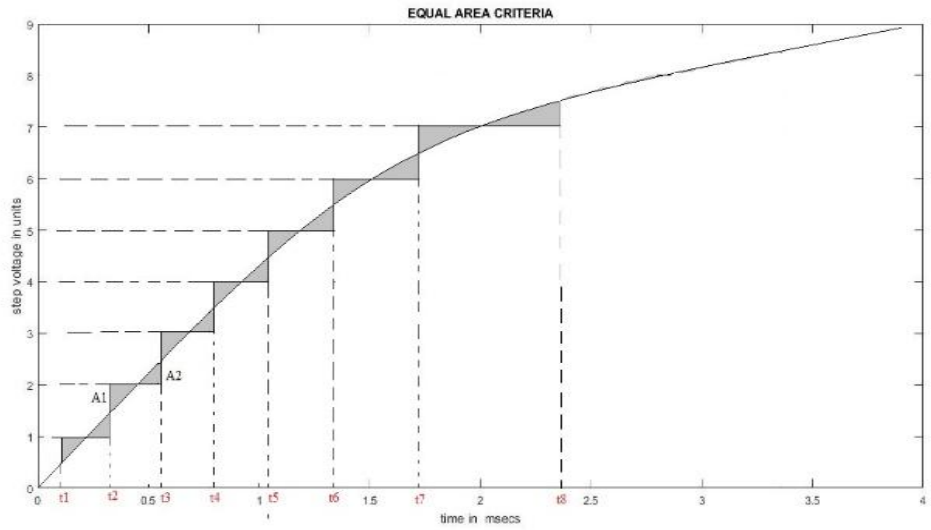

Fig.4: Modulation Techniqueof Equal Area Criteria:

Equal Area Criteria:

This method tries to calculate the switching angles such that to reduction in theharmonic content of the output voltage in multilevel inverter, it is totally different approachas this method no need of solving the high-order multi-variable polynomial equations like Newtonraphson method.

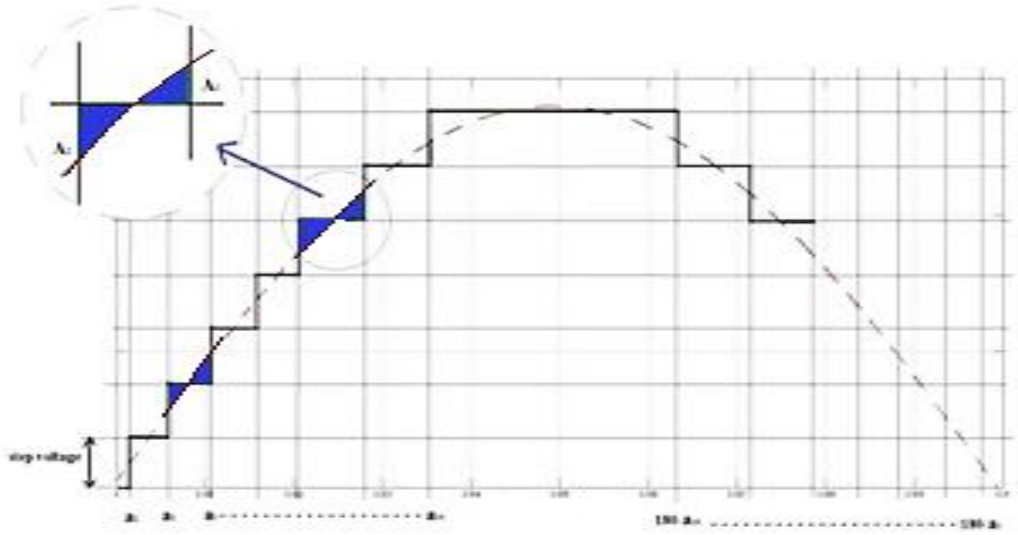

Fig.5: Equal Area Criteria (EAC) switching technique

In this method we can calculate the best switching angles by dividing half of fundamental sine wave (frequency of 50Hz) horizontally and vertically with step voltage along the y-axis and time in (m-s) along the x-axis respectively. The horizontal and vertical lines are drawn in such way that the areas of A_1 and A_2 are equal to get minimum total harmonic distortion (THD). The fundamental switching frequency is taken as 50Hz, the stepvoltage is a minimum

voltage that connected in level generation cell (LGC) in the topology. If a_1, a_2, a_3, $a_n$are the switching angles for N-level inverter topology then total angles should be less than 90^0.

i.e. 0<a1 <a2<a3<a4<a5<a6<a7 - - - - an<90^0

Number of switching angles required for N-levels = [(Number of levels-1)/2].

Mathematical formula forswitching angle calculation:

N^{th} switching angle in (deg.) = [[Time at which the N^{th} level vertical line touches the time axis (x-axis)]*[2*fundamental frequency]]*180^0.

Using this mathematical formula for N-number of levels the switching angles can be calculate. The switching angles for 17- level inverter topology using equal area criteria from the fig 5 are

$a_1=5^0$, $a_2=19^0$, $a_3=37^0$, a4=$56^0$$a_1=2^0$, $a_2=9^0$, $a_3=16^0$, $a_4=24^0$, $a_5=32^0$, a6=41^0, $a_7=53^0$, $a_8=66^0$

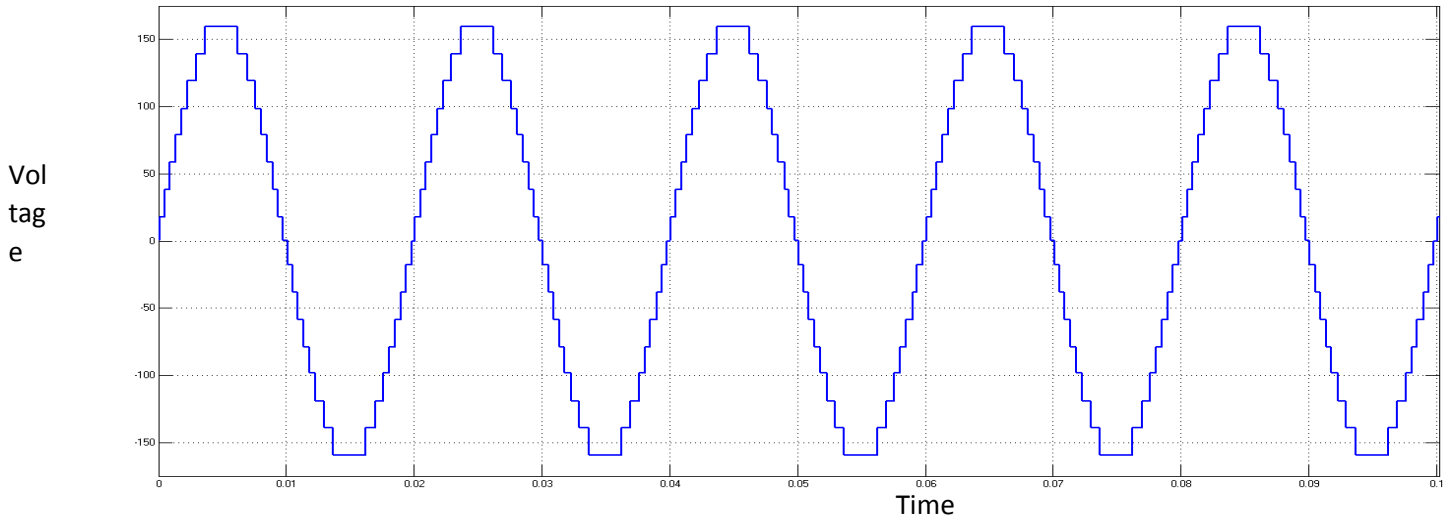

Figure 6: Output voltage waveform of 17-level (y-axis=20V/div. x-axis=10ms/div.)

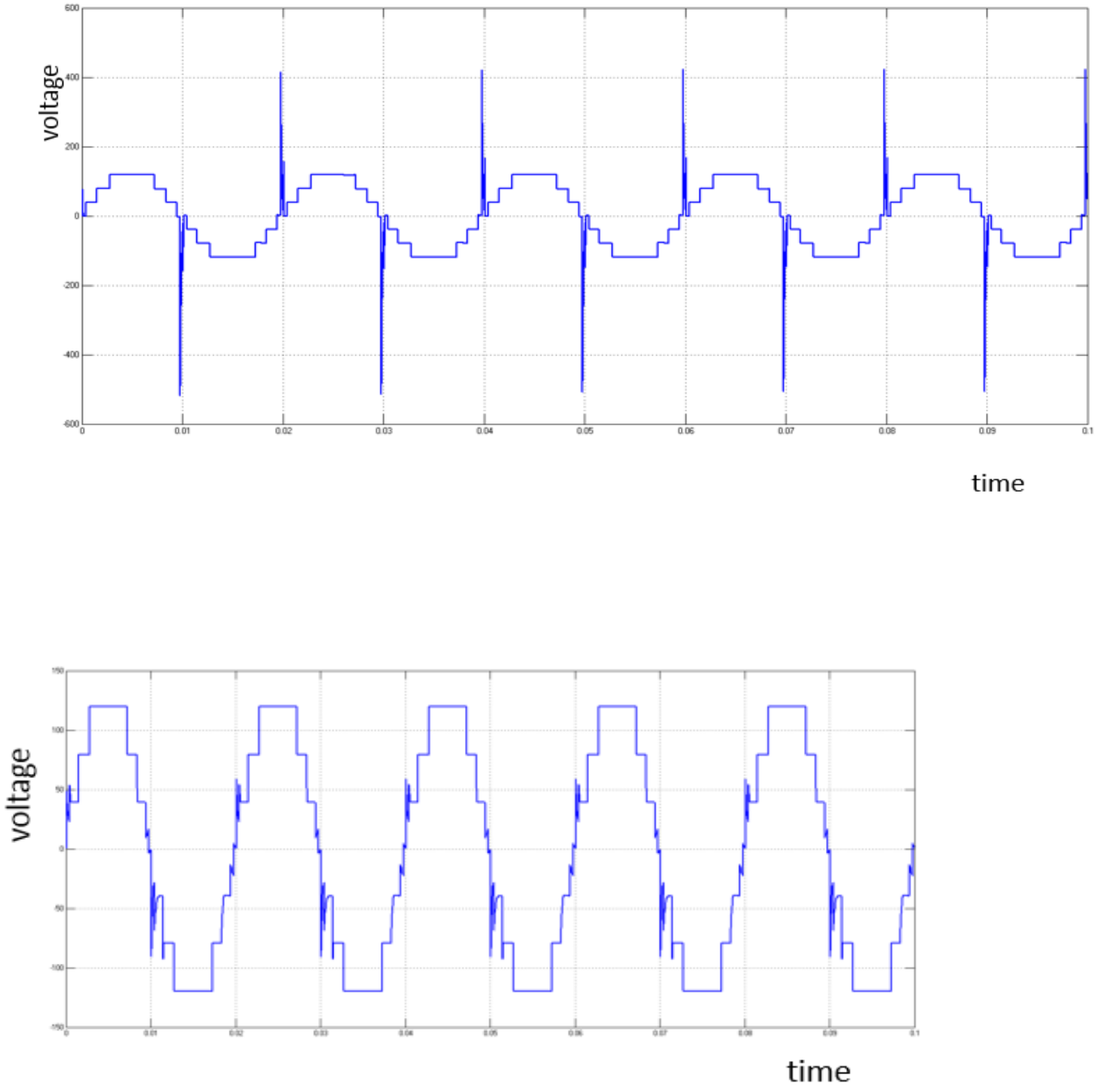

Fig 7: 7- level Inverter output voltage with inductive load (R-L)

Fig 8: 7-level inverter output voltage forms with RL-load and external circuit resistance

Comparison of Total Harmonic Dissertation for different inverter topologies

Consider the 7, 9 and 17 level inverter topologies with the inductive (R-L) load, results in a very high magnitude of the output voltage at zero crossing. This will cause the damage the

switching device and also the inverter system. The magnitude of voltage spikes can be reduce at zero crossing by increasing the number of levels of the inverter topology.

At zero crossing the magnitude of voltage spikes is very high due to the energy stored in the inductor. The stored energy in the inductor can be dissipated through the antiparallel-diodes which are the body diodes of the switching device (MOSFET). This can be possible when 2-switches of H-Bridge are turn ON at zero crossing (i.e. either the upper two switches or the bottom two switches), so the inductor current needs sufficient time duration for dissipating stored energy at zero crossing , this is possible with less number of levels but THD is more and presence of voltage spikes . But using this technique there is decrease in magnitude of voltage spikes about 86.66% in 17-level inverter topology with the R-L load that shown in fig.10.So the 17-level inverter topology is suitable for R-L load.

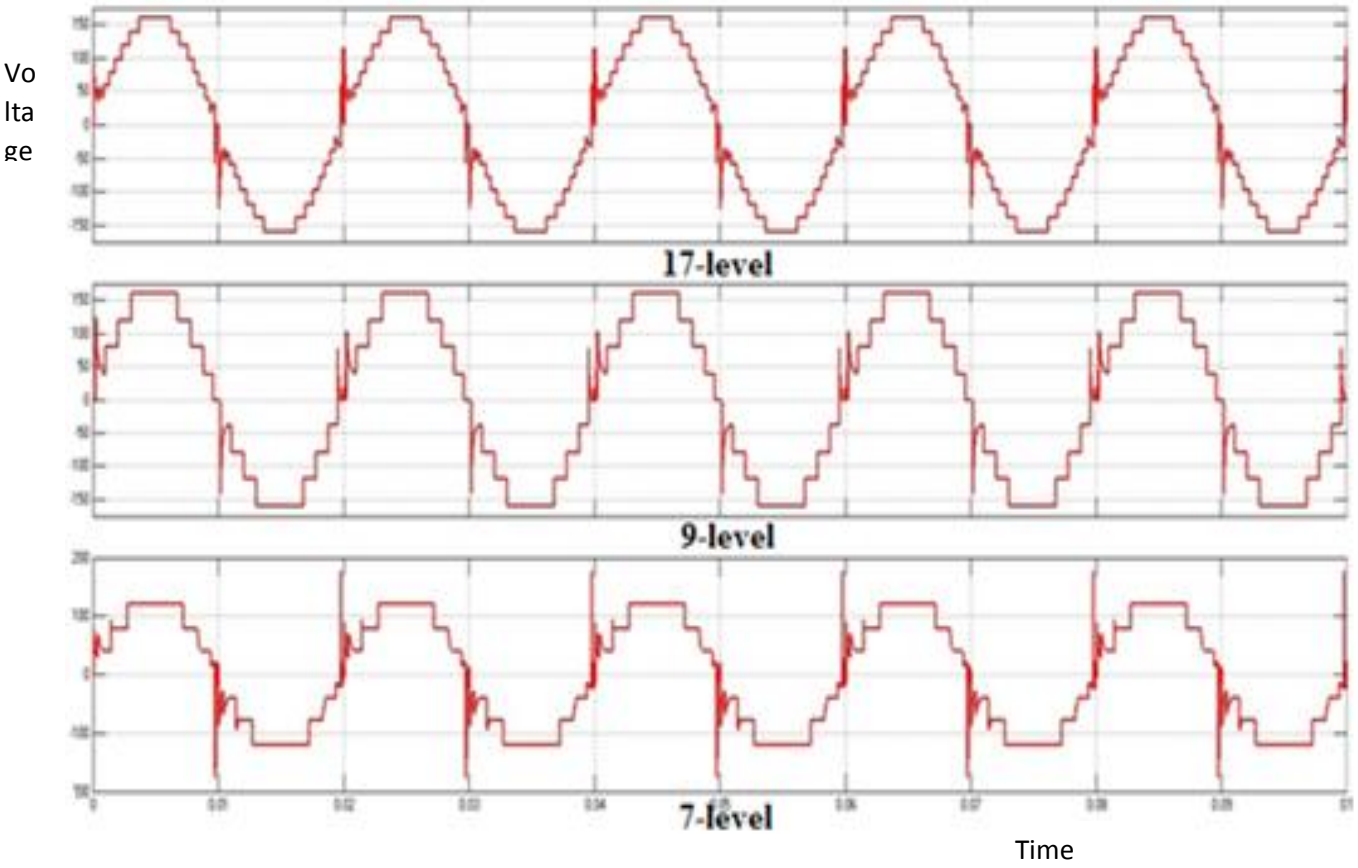

Fig 10: Output voltage waveforms of 17, 9 and 7 level inverter with Inductive (R-L) load

CONCLUSION

This paper focuses on 7, 9 and 17 level inverter topologies with harmonic analysis for inductive (R-L) load, the voltage spikes at zero crossing with high magnitude due to energy stored in the inductor. This voltage spikes magnitude can be reduced either the upper two switches or bottom two switches of the polarity generating cell (PGC)of about 86.66% it has

been performed by using MATLAB SIMULINK which verifies that 17 level multilevel inverter is the best suited topology for R-L load.

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