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RFIC Implementation Feasibility for Space System Miniaturization

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***Abstract*—The main aim of this paper is to introduce RFICs (Radio Frequency Integrated Circuit) in the field of receiver, and having a thorough study of its feasibility in this field. The design flow and implementation aspects are being studied, also the various kinds of available technology are being put forward. The SiGe technology for RFIC is put forward with its significance for space application .The RFIC implementation scope in command receiver analyzed.**

***Index Terms*— RFIC (Radio Frequency Integrated Circuit), SiGe (Silicon Germanium), GaAs (Gallium Arsenide), CMOS (Complementary metal oxide semiconductor)**

I. INTRODUCTION

RFIC is one of the emerging technologies in the field of integration. Integration provides a means of significantly reducing the size and weight of the product. The total number of components used in a system is also reduced, which will improve the system yield and reliability. In many portable communication products available today, the vast majority of IF (Intermediate Frequency) and baseband circuitry are integrated. However, in many cases discrete components are still used extensively throughout the RF section.

The Table below compares the main parameters of the discrete implementation to the integrated one:

Parameter	Discrete	Integrated
Development cost	Moderate	Very high
Modifications	Relatively easy and inexpensive	Expensive, generally one or more new masks
BOM cost	Low	Depends on volume, die size and process used
Mixing technologies	Optimum device technology can be used throughout	Limited scope
Parts count	High	Low to very low
Size	Small to medium	Smallest
Weight	Light	Lightest
Cost of using additional transistors	Moderate	Low
Matched transistors	Difficult to use effectively	Very good, used extensively

Table.1

The main reasons for the extensive use of RFIC's in today's era (especially in wireless industry) are:

1) An increasing number of RFICs offering acceptable performance at a competitive price, are now becoming commercially available.
2) Product design times can be shortened if suitable integrated circuits are available, since discrete versions need not be developed
3) The use of ICs allows reduced size and weight.

Considering the RFIC's impressive features, mainly reduced size and weight its feasibility to be used in satellite communication receiver application is being undertaken. To start with, the feasibility of realizing IF portion of the C-band receiver is taken up in RFIC.

II. CONSIDERATIONS FOR RFIC DESIGN

A. *Level of Integration*

When choosing to integrate RF circuit, decisions must be made to what level of functionality should be integrated onto a single die. Whilst the highest possible level of integration may offer largest reduction in size, weight, and component count, it may not offer best technical solution. Problems may occur because of on chip cross- talk or the effects of packaging parasites may unacceptably degrade the rejection provided by the external filters. The consequences of integrating different circuit functions very close together on the same chip must be considered. Another factor, which must be considered, is the die size. A wafer of ICs will cost the same to fabricate whether it contains 10000 circuits or 100 circuits. Clearly the larger the circuit occupies, the more expensive the die. This is compounded by the fact that larger die will also exhibit lower yields.

B. *Active Biasing*

Discrete RF circuits normally utilize inductors and/or resistors to inject the drain/collector bias and resistors to inject the gate/base bias. While simple control loops are sometimes used to set up the bias current, additional active devices mean additional cost and generally the number of transistors used is kept as low as possible. With ICs, additional active devices can be used with minimal cost implications. Indeed, passive components normally occupy more die area than active, particularly at lower frequencies. This results in active biasing techniques being used on wider basis.

C. *Crosstalk*

Crosstalk is the interference of a signal due to the unwanted coupling of energy from a different signal. It is reduced by shielding, de-coupling and physical separation. If two

different signals are present on the same die there will be cross-talk. The unavoidable close proximity of circuits fabricated on the same die means that cross-talk will always occur whenever multiple signals are simultaneously present. Reducing the level of cross-talk once the die has been fabricated is not practical. So, while designing care should be taken to avoid the cross-talk.

D. Differential Circuitry

A benefit that differential, or balanced, signals have for the use in RFICs is that they are not referenced to the PCB ground and do not require low inductance RF grounds. Differential circuits have "virtual earth" points, where the differential voltage cancels the DC bias and ground return points can be conveniently connected to these points. The ground return paths should have low DC impedance but high RF impedance. Single-ended or common mode, signals are referenced to the PCB ground and will be rejected by the differential circuitry. The higher the impedance of the ground return, the better the common mode rejection.

In summary, the use of differential circuitry offers the following advantages:

1) Immunity to common lead inductance problems.
2) DC bias can be injected at "virtual earth" points without the need for low impedance RF grounds.
3) Rejection of interfering common mode signals.
Differential Circuitry

E. Through Substrate Vias

Many processes allow the fabricating through substrate via holes. These offer means of realizing low inductance connections to the back of the die, which is normally the ground. The facility greatly eases the design process. Without it, all points which must be RF grounded need to be taken to pads at the edge of the die and bonded to ground. Despite the benefits of through substrate vias, designers of ICs should avoid using them as it is an additional process step and is normally time consuming and costly to perform.

F. Packaging

The main packaging effects that should be considered:

1) Series inductance to RF input/output ports
2) Common lead inductance between RF ground of the die and the PCB
3) Coupling between package legs
4) Dielectric loading as a result of the plastic covering of the die.
5) Loss loading as a result of the plastic covering of the die
6) Increase in junction to ambient temperature.

III. RFIC DESIGN CHALLENGES

In general, for the technologist as well as the circuit designers the challenges here are:

1) To make the transistors operate at higher frequencies
2) To integrate as many as components required in the receiver onto the IC.

The key factors for optimization are

1) Increased density
2) Reduced power consumption

The design of RFICs is considerably more complicated than that of microwave ICs in GaAs or the other III-V semiconductor technologies. RFICs typically employ large number of devices and include RF, DC, and digital functionality. Routing and parasitic extraction technologies are essential, as are methods for characterizing distributed elements on lossy substrates. Important performance specifications in RFIC are noise, linearity, and gain RF circuits need passive components viz. resistors, capacitors, and inductors. In many cases the overall performance is determined by the passives. It is very important to have high quality passive components.

IV. RFIC TECHNOLOGY

A. Trends in RFIC Technology

Here, some insight is put into the current trends in the RFIC field. There is wide range of possibilities: CMOS, Bi-CMOS, GaAs, Silicon Bipolar, SiGe. CMOS and Bi-CMOS is widely used in the wireless design, the key driving force is the low cost with some optimized performance. The factors that contribute to the significantly lower cost of circuits manufactured on Silicon substrates compared with other semi-conductor materials GaAs and SiGe:

1) Processes for CMOS and BiCMOS circuits provide higher yields
2) The high volume of orders in CMOS fabrication facilities helps reduce the cost of such circuits through economics scale.
3) Analog circuits implemented in CMOS can be really integrated on the same substrate with the digital baseband processing circuits for a truly single chip implementation of the system.

B. Technology Selection for RFIC

The technology choices in Silicon are CMOS, Bi-CMOS and Bipolar, while the technologies available in GaAs are MESFETS, HBT, p-HEMT. What differentiates between circuit families on the same semiconductor are the masking steps, the levels of doping used in the realization of the transistors and the manner in which the transistors are created and used. For example the bipolar transistors available in a BiCMOS process are inferior to those available in a dedicated silicon process. The RF designer's choice of a circuit family is driven by the desire to meet the objectives for:

1) Low power dissipation
2) Speed
3) Yield
4) Component noise
5) Linearity
6) Gain
7) Efficiency

To date, there is no single family that can simultaneously meet all these requirements at RF, IF and baseband. Baseband analog circuits for implementing filters, amplifiers, and A/D and D/A's are dominated by CMOS.IF circuits such as mixers, amplifiers and some filtering operations are realized in a mix of CMOS, BiCMOS and Bipolar technologies. Finally, power amplifier and LNA functions are generally realized in GaAs. The Table.2 shows a comparison of the various technologies.

Keeping in mind the application, which is more performance oriented, Silicon Germanium technology was the selected. SiGe HBT technology combines transistor performance competitive with III-V technologies with the

processing maturity, integration levels and yield hence, cost commonly associated with conventional Si fabrication.

Table.2

	GaAs	*SiGe*	*Si bipolar*	*Si CMOS*
High cut-off frequency-f_T	XXX	XXX	XX	XX
Low noise	XXX	XXX	XX	X
Good isolation	XXX	XXX	XX	X
Good passive components	XXX	XX	X	X
Low power consumption	X	XXX	XX	XX
Low voltage operation	X	XX	XX	XX
High level of integration	X	X	XX	XXX
Low cost	X	X	XX	XXX

XXX - Excellent
XX - Very Good
X - Good

V. Silicon Germanium Technology

The silicon-germanium hetrojunction transistor (SiGe HBT) is the first practical bandgap-engineered device to be realized in silicon. SiGe HBT technology combines transistor performance competitive with III-V technologies with the processing maturity, integration levels, yield, and hence ,cost commonly associated with conventional Si fabrication. State-of-the-art SiGe HBT's technology can deliver :

1) f_T in excess of 50 GHz
2) f_{max} in excess of 70 GHz
3) 1/f noise corner frequencies below 500GHz
4) Minimum noise figure below 0.7 dB at 2.0GHz
5) Excellent radiation hardness
6) Cryogenic operation
7) Competitive power amplifiers
8) Reliability comparable to Si

A host of record-setting digital, analog, RF, and microwave circuits have been demonstrated in the past several years using SiGe HBT's and recent work on passive and transmission lines on Si suggest a migratory path to MMIC's is possible. The combination of SiGe HBT's with advanced Si CMOS to form SiGe-BiCMOS technology represents a unique opportunity for the Si-based RF system-on-chip solutions.

A. Si Engineered to develop SiGe

We live in silicon world. Greater than 95% of today's global semiconductor market uses the semiconductor silicon to host of integrated circuits. This profound market dominance of Si rests on number of surprisingly practical advantages Si has over the other numerous semiconductors, including:

1) An extremely high quality dielectric (SiO_2) can be virtually grown on Si and used for isolation, passivation, or as an active layer (eg.gate oxide)
2) Si can be grown in very large, virtually defect-free single crystals, yielding many low-cost IC wafer.
3) Si has excellent thermal properties allowing for efficient removal of dissipated heat
4) Si has excellent mechanical strength, facilitating ease of handling and fabrication.
5) It is easy to make very low-resistance ohmic contacts to Si, thus minimizing device parasitic.
6) Si is easily available and easily purified.

Yet from the designer's viewpoint, Si is hardly the ideal semiconductor. The carrier mobility for both electrons and holes in silicon is rather small, and the maximum velocity that these carriers can attain is limited to about 1x 10^7 cm/s under normal conditions. Since the speed of device ultimately depends on how fast the carriers can be "pushed" through the device under practical operating voltages, Si can be regarded as somewhat "slow" semiconductor. In addition, because Si is an indirect gap semiconductor, light emission is inefficient, making optical devices such as lasers impractical.

Many of the III-V compound semiconductors (eg.GaAs, InP), on the other hand, enjoy far higher mobility's and saturation velocities and, because of their direct band gap nature, make excellent optical devices. In addition III-V devices, by virtue of which they are grown ,can be compositionally tailored for a specific need of application. This "band gap engineering", as it is known, yields a large performance advantage for III-V technologies.

These benefits commonly associated with III-V semiconductors pale in comparison to the practical deficiencies associated with making highly integrated low-cost IC's from these materials .Few reasons for this are:

1) There is no decent grown oxide for GaAs or InP.
2) Wafers are smaller with much higher defect densities, more prone to breakage, poorer heat conductors.
3) These translates into lower levels of integration, more difficult fabrication, lower yield , and ultimately higher cost.

While the idea of using SiGe alloys to bandgap-engineer Si devices dates to the 1960's, the synthesis of defect-free SiGe films proved quite difficult, and the SiGe films were not successfully produced not until the early to mid-1980's.While Si and Ge can be combined to produce chemically stable alloy, their lattice constants differ by roughly 4% and, thus SiGe alloys grown on silicon substrates are compressively strained. This is referred as "pseudomorphic" growth of SiGe on Si.

Introducing Ge into Si has a number of consequences,

First and the most importantly, because Ge has a larger lattice constant than Si, the energy bandgap of Ge is smaller than that of Si(0.66 eV versus 1.12 eV), and thus we expect SiGe to have bandgap smaller than that of Si. The compressive strain associated with SiGe produces additional bandgap shrinkage, and the net result is a band gap reduction of approximately 7.5 meV for each 1% of Ge introduced.

This Ge-induced "band offset" occurs predominantly in the valance band, making it conductive for the n-p-n bipolar transistors. In addition, the compressive strain lifts the conduction and valance band degeneracies at the band extremes, effectively reducing the density of the states and improving the carrier motilities with respect to Si.

B. Radiation Tolerance of SiGe

An important emerging market for RF and microwave circuit is in space-born satellite systems, key components in the requisite infrastructure to support global communications networks for voice, video, and data transmission. *Space is an amazingly hostile environment, due not only to the extreme temperature encountered between solar shade and solar illumination, but importantly from a radiation stand point.* The temperature extremes can be dealt with when needed by adding heating and cooling systems, but the impact of radiation is much more severe since effective shielding of sensitive electronics from high-energy particles is impractical (it is hard to launch a satellite with two feet of lead shielding). Depending orbital position and altitude, satellites are routinely exposed to large and potentially lethal fluxes of high energy protons, neutrons, electrons and gamma rays (high-energy photons). *Given the cost of building and launching of satellite, radiation induced failures can be tolerated. For this reason, space-borne electronics are subjected to exhaustive radiation testing, and usually require very costly "radiation-hardening" process, layout, and circuit design modifications before they can flow in space.*

The "holy grail" in this context is to have a *standard* (terrestrial) *device technology which can be inherently radiation-hard as fabricated and, hence, space qualified without any process of modification. Preliminary suggest that this is the case for SiGe HBT technology with respect to gamma rays, neutrons and protons as shown in the fig1, both before and after exposure to 46-MeV protons at fluences ranging from 10^{12} to 10^{14} cm^{-2} (10^{14} cm^{-2} is a higher fluence encountered in practical orbits).*

For proton fluences upto 10^{13} cm^{-2} only minor drifts in base current are observed and negligible degradation in frequency response occurs. The impact of extreme radiation exposure of protons, neutrons, and gamma rays on the β of the SiGe HBT was studied and, as expected proton irradiation has more serious impact on device operation, since it produces both displacement damage and ionization damage.

This radiation hardness in SiGe is because of the device structure. From radiation immunity view point the SiGe HBT structure has several intrinsic advantages:

1)The EB spacer is very thin and composed of radiation-hard oxide-nitride composite
2) The extrinsic base doping under the EB spacer is very high, effectively confining any ionization damage in the region.
3) The active device region is very thin and, hence, the total volume exposed to particle displacement damage is minimal.
4) The deep and shallow trench isolation minimizes the exposure of oxides that can contribute to junction leakage temperature.

C. Temperature Effects on SiGe

Bandgap engineering has a very positive influence on the temperature characteristics of SiGe HBT's and thus allows the SiGe to operate well in the Cryogenic environment (eg. Liquid – nitrogen temperature = 77K).The frequency response of SiGe which can be explicitly optimized for 77K operation. At 84K, this SiGe has an output current drive greater than 1 $mA/\mu m^2$, a peak β of 500, a peak of 60GHz, and the peak f_{max} of 50 GHz , all significantly higher than 300K

VI. RFIC Design flow

A proper design flow should be followed for RFIC, given the speed requirement, as this makes circuits extremely sensitive to parasitics, including parasitic inductance, passive modeling as well as noise. Thus, *the essence of the RFIC flow is the ability to manage, replicate, and control post layout simulations and effectively use this information at timely points through the design process.*

IC design also requires analysis techniques that are specific to RF design. The cross between frequency and time domain analysis methods, which are chosen on the basis of circuit type ,designer comfort level, circuit size or designer preference. Ultimately this requires a seamless environment that that facilitates the choice of requirement.

Typical requirements that a complete design flow needs to support are:

1) Enabling Top-Down and Bottom-Up design
2) Fast architectural exploration for optimized RF specifications
3) Complete application –specific test benches
4) Comprehensive consideration of parasitic effects.
5) Verification at system level at each stage.

The three main parts identified within the proposed solution are:

1) RF architecture selection and optimization
2) Verification and exploration at system level
3) RFIC implementation and Verification at system level at each stage.

To explain it in a better manner, for the RF architecture to be optimized, then the first stage is to realize transistor-level circuits for the blocks of the actual architecture. Based on the block specification topology and the ranges for independent variables (size of devices, currents, voltages, etc),multiple simulations have to be done during the sizing process, and later on, the designer should analyze trade-offs between goals and sensitive design variables.

Due to higher frequencies and higher integration, passive components (package, transmission line, spiral on-chip inductors etc.) become more and more important in RFIC's process .There are various ways to model/characterize these components (modeling based on formulas or look-up tables, electromagnetic field simulations, and/or measurements).The results are always RLC lumped-element models and/or simulated /measured S-parameter data that could be used with circuit simulation.

Similar to passive component modeling, a comprehensive consideration of parasitic effects is absolutely mandatory .Especially substrate coupling and inductive nature of interconnects are of vital importance in designs.

To sum up, for optimized design flow we can have the top-down and bottom-up processes working in parallel producing a *"meet – in – the – middle"* approach. It is this *"meet – in – the – middle"* approach that balances the need for speed through the design process and silicon accuracy, ultimately producing a predictable schedule leading to first pass success.

A. Foundry for SiGe

Foundries for RFIC are very important for an integrated functionality. The first step towards this is selecting a foundry to work with. This is done at the earliest, since there

are many variables in process technology, available design tools, manufacturing capacity, and technical support.

A key design issue is the simulation technology supported and verified by each foundry. Although most EDA tools are supported by all foundries, there are preferences for each, based on the level of cooperation between the software developers, their customers and foundries.

Another issue in RFIC design is the match between the RF circuit design and the available transistors and passive devices available for each process. Each foundry will have model will have its own devices, which must be used in the creation of the circuit. The limitations of the component types, range of values, currents, voltages and device performance must be considered in the initial RF "block diagram" design.

B. Automation Tools for Design

The EDA tool for RFIC design plays a very important role for an efficient design management. The RFIC design tools must incorporate efficient methods for analyzing circuit behavior, accurate semiconductor models and flexible system modeling. The accuracy of a simulation is dependent on three factors:

1) The accuracy of the models
2) The error caused by the simulator algorithms, and
3) The circuit set up itself.

Before starting the design the foundry kit called the *Process Design Kit(PDK)* should be loaded in ADS. Design Kits consist of symbols for each device that are linked to its device model and layout (as shown in the figure below). PDKs cover the entire design procedure from schematic entry, simulation, layout, to post simulation.

VII. RFIC IMPLEMENTATION SCOPE IN COMMAND RECEIVER

Of the various schemes available for the receiver the traditional Double down conversion is extensively used. It has been a dominant choice for the major advantages of:

1) Superior performance with respect to selectivity and sensitivity.
2) Its adaptability to many different receiver requirements.

For the present ongoing GEOSAT mission's C-band and Ku- band command receivers are used as per mission requirement. The RF front end being at microwave frequency RFIC not a feasible option as we may have to forgo many performance parameters while designing RF front end with RFIC.As performance for space application is at premium, thus RFIC at front end not considered. The various mentioned receivers for GEOSAT has its IF at around 200MHz to 1000MHz ,for which RFIC based IF down conversion becomes an ideal solution for system miniaturization. The main aim to replace the IF segment, which consist of amplifiers, SAW filters and mixer with an SiGe RFIC. In the present receiver scheme, the various filters have to be kept outside, as this provides greater flexibility in the frequency band of operation and reduction in size.

VIII. CONCLUSION

The RFIC technology feasibility for radiation hardened space application has been studied and SiGe was found to be suitable for space application. The IF stage is found to be suitable for RFIC implementation of the receiver Downconverter, the design will be taken up for RFIC design on SiGe with appropriate process selection.

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