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Design and Implementation of an SRAM based 4X5 Ternary CAM using Reversible Logic

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Abstract— **Reversible logic is a style of computational process there exists a one to one mapping with inputs and outputs. Content addressable memory (CAM) is a special type of memory classified into two. Binary CAM & Ternary CAM. This can be used in place of Random Access Memory (RAM) that finds its use in mobiles, computers etc. Especially, this memory finds its application in CISCO routing switches. Binary CAM can perform search operation like a look up table in a single clock cycle. But it suffers the drawback of high power dissipation during the matching operation. Ternary content addressable memory (TCAM) performs searching based on three logic values viz., logic 0, logic 1, logic 'X'. A the demand for high speed internet is increasing day by day, attention has been focused on TCAMs as a key device for increasing the speed of packet forwarding (packet data transfers) by networking equipment by enabling high speed lookup of destinations, etc., for large volumes of information during packet data transfers. Reversible logic has also gained its interest from the recent past because of its ultra low power characteristics. This paper deals with the design and implementation of a 4X5 TCAM using reversible logic with the target device being the Xilinx Spartan 3E FPGA. The proposed design utilizes conventional SRAM operation executed by reversible logic version of SRAM. The design is well optimized in terms of quantum cost and number of garbage outputs.**

Index Terms— **Content Addressable Memory, TCAM, Quantum Cost, Garbage Output, Power Consumption, Reversible Logic**

I. INTRODUCTION

Some superior systems make use of an extra-ordinary sort of memory known as Content-Addressable-memory that is different from the Random Access Memory. They are denoted as CAM and RAM all through the parts. Usually in RAM, a working frame work must utilize the memory delivers to get the information put away at this address area. Where as a CAM works in an inverse way, that means working framework must utilize the information put away and then CAM work is to deliver the address area in the memory where the information is found. At a given moment RAM can get to just a single area where as a CAM can get to the whole memory areas and hence it is clear that CAM is nearly quick memory than RAM.

Planning a CAM is complex and even costly to build. In addition to it CAM requires much power creates warm into the framework amid rapid controls. CAM has a drawback of high power scattering amid the coordinating what's more, seeking substance.

The CAM is also known as a double CAM as it works with just two states rationale '0' and rationale '1' and hence can be used for correct coordinating esteems. TCAM, the enhanced variant of CAM, which stands for Ternary Content Addressable memory have the working states as rationale '0', rationale '1' and rationale 'X'. 'X' signifies the estimation of obscure state. The TCAM is capable of utilizing the third state as the veil bit to control which bit is to be coordinated and which to be disregarded as couldn't care less or obscure state.

The superior steering systems and types of gear dependably use TCAM consolidated it into high useful steering tables and uncommon kind of query work tables. To outline such a TCAM cell numerous systems were into the plan business. As the speed of operation of the TCAM memory is high, bigger calculations should have been completed rapidly but there might be a chance of losing the data. This losing of data might result in the age of parcel of warmth into the framework.

To overcome this, we make use of the circuits planned with reversible-rationale components on the grounds that the reversible-rationale circuits have been demonstrated in an ideal world with zero scattering of warmth into it. Later we used the reversible-rationale gates to plan the TCAM cells to limit the dissemination of warm in it. This proposed strategy includes the plan of 5 bit wide 4×5 TCAM cluster using reversible sort gates and further it introduces the 4×3 TCAM cluster along with the basic TCAM cell. An SRAM cell is also similarly planned with reversible articles for putting away information bit in the TCAM cell. Along with the reversible gates the match-line and the inquiry line are additionally acknowledged. This proposed plot combines a few reversible-rationale gates like Feynman Gate, Fredkin Gate and Peres Gate. These entire modules are examined and reenacted with the help of Xilinx ISE test system.

II. LITERATURE SURVEY

In this chapter, we discuss about the information found by study and research that is critical and have an important value in the contribution of the whole paper. It also gives a basic knowledge or provides a theoretical base to successfully achieve the main objectives. Most of the literatures are from the related articles, journals, books and previous works of the same fields. These literatures are then compiled and used as a guidance for this paper. There are two interesting things that result while outlining any combinational or successive circuit plan. The principal thing is streamlining the speed of operation of any circuit and the second one is method to upgrade the variables which influence control use by these

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rapid circuits. In the faster system circuits, uncommon sort of memory components like TCAM is required for more extensive pursuit and in addition rapid inquiries .In the cutting edge days the reversible- rationale sort configuration is used as it is having ultra most minimal power designs. To overcome with control issues while planning any low power circuit, we should utilize the reversible-rationale components.

As per Prashant R.Yelekar[1], to understand the Boolean capacities the reversible-gates can be useful in every general circuit. He has introduced ideas for some imperative reversible gates, namely, Fredkin gate, Feynman gate, Toffoli gate and Peres gate. He has utilized these gates to fabricate the perplexing circuits including both combinational and successive circuits. Nagarjuna S [2] and some others proposed an idea that the memory components utilized as a part of RAM like D flip-slump and RS flip-tumble are additionally planned by utilizing the reversible gates. Their proposed plans were purchased relatively better comes when compared with the current ones. The main motive behind their outline is to lessen the power by improving the gate parameters such as quantum cost, number of junk yields and profundity of the circuits.

Mathew Morrison [3] and some others proposed the outline of SRAM and DRAM that exhibits the use of reversible- gate and decoder. They additionally exhibited a MLMR gate which was used for controlling the perused/compose operations in SRAM cell. Shailja Shukla [4] and some others proposed a most reduced handling unit convey look forward snake utilizing reversible articles what's more, outline was reenacted utilizing Micro- wind 3.1 reproduction apparatus on 90nm scale innovation. They got configuration that was enhanced with 47ns deferral, 0.2 mw control devoured and 245µm2 range gained. A novel on quantum-cost-proficient reversible full-snake gate in nanotechnology was introduced by Md. Saiful Islam [5]. Here the gate can be an all inclusive gate which that implies it is utilized for blending any Boolean capacities. Ordinarily this gate is alluded as the Peres Full Adder Gate.

A CAM chip exhibited by Dejan Georgiev [6] is outlined at design level. He has also introduced two power lessening strategies, the first one is pipelined-control plot and the second one is adjusted pre-calculation based approach. A SRAM based engineering for TCAM proposed by Zahid Ullah [7] and some others have utilized the advantages of SRAM to outline Z-TCAM. They have outlined two models of size 512×36 and 64×32. These inclinations and methods help us to plan a quality level outline with effective outcomes. These rising strategies for current planning enhance our abilities of outlining and lessen the plan exertion.

III. REVERSIBLE ELEMENTS

Among the reversible and irreversible-rationale gates, utilization of irreversible gates dependably scatters warm into the earth. Yet, with the use of reversible-rationale gates we accomplish zero warmth dissemination in a perfect world. A rationale gadget is said to be reversible in the event that it has square with number of sources of info and yields and must have balanced mapping between them. By using conditions of yield variations the conditions of the information variations can be reproduced. This property guarantees sensible reversibility as the information sources and yields can be retrievable from each other remarkably. The primary topic of the reversible-rationale orchestrating is to manage the underneath said parameters.

- Minimize waste yields of the circuit.
- Reduce number of gates in the circuit.
- Minimize the extra sources of info that are not required.
- Minimize the postponements in the circuit.
- Decrease the circuit's quantum taken a toll.

There are various types of reversible-rationale gates like Toffoli Gate, Feynman Gate, Fredkin Gate, Peres Gate and a few others. Among these Feynman Gate, Fredkin Gate and Peres Gate are used as a fraction of the future plan modules. A Brief discourse about these reversible gates as tails one by one. Each gate is having its exceptional usefulness for outlining the unique modules required for the proposed plot.

A. 2X2 Feynman Gate

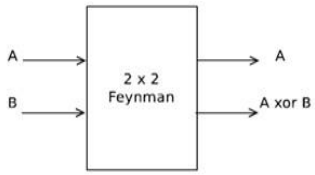

Fig.1. 2×2 Feynman Gate

The figure 1 demonstrates the 2×2 Feynman gate with inputs 'A' and 'B' and yields 'A' and 'A XOR B'. The Feynman gate can be used as XOR Gate and in addition it can be utilized as a NOT Gate. It is likewise utilized for duplicating its yield to the following gate as it is a fan-out gate. Its quantum cost is 1.

B. 2X2 Fredkin Gate

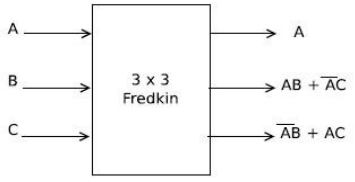

Fig.2. 3×3Fredkin Gate

Figure 2 demonstrates the 3×3 Fredkin gate with inputs 'A', 'B' and 'C' and yields 'A', '~AC XOR AB' and '~AB XOR AC'. The Fredkin Gate can likewise be utilized as a choosing gadget for products with input 'A' as a select line. The quantum cost is 5

C. 3×3 Peres Gate

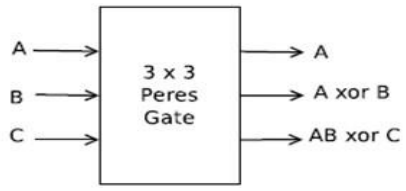

Fig.3. 3×3Peres Gate

The figure 3 demonstrates the 3×3 Peres Gate with inputs A, B and C and yields A, (A XOR B) and (A AND B) XOR C. The Peres Gate preserve be a match-line also be an inquiry line by Fredkin Gate. Quantum cost (QC) of this gate is 4.

D.Basic SRAM Cell

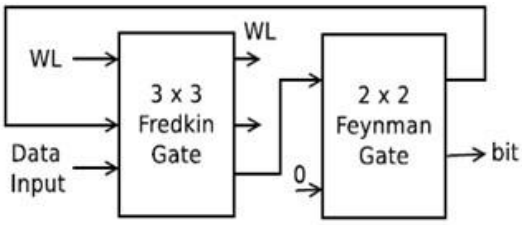

Fig.4.Basic SRAM Cell

The figure 4 demonstrates the basic SRAM cell composed of Fredkin and Feynman gate. This SRAM cell is used to store single bit an incentive in TCAM cell. In the fig,'WL' i/p is a word- line which make SRAM cell to work also in read/compose state. In the event that WL=0, at that point it holds the past esteem. This overall quantum cost (QC) is 6.

E. Content Addressable Memory

Binary CAM, in short Bi CAM is a content addressable memory with high speed data search capability. To understand the functionality of CAM, it is generally compared with RAM used in mobiles, laptops, desktops etc. In order to search data already stored in RAM, we should provide the address of the data needed to be extracted from it. IN contrast with RAM, data stored in CAM can be searched by using search keyword as the data itself and the CAM returns the addresses that match with the data searched for. The specialty of CAM is that, entire location can be searched in just one clock cycle. Hence this type of memory is much faster than the classical memory (RAM).

IV. PROPOSED ARCHITECTURE

The very disadvantage of this type of memory (BiCAM) is that it can perform the search and give fruitful results only when the search data exactly matches the stored data in one or more location. Simply saying, it uses the exact match search algorithm to extract data from it. And as the name implies, it accepts either a '0' or '1' state. To overcome this problem, our proposed architecture employs Ternary Content Addressable Memory (TCAM). Ternary means three and as the name suggests, TCAM accepts logic '0', logic '1' and don't care condition 'X'. Exact match of the content/ data is not necessary for TCAM to perform search operation. Even a small match of the data is sufficient. All the relevant data with

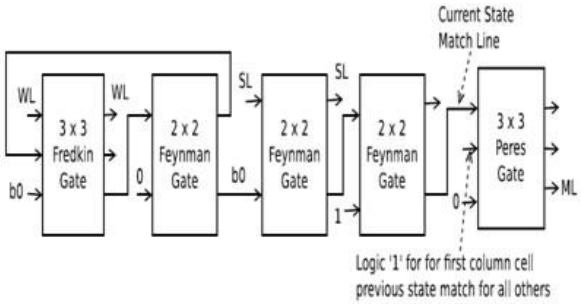

Fig.5. Basic TCAM Cell using Reversible Logic

that minimal match will be retrieved in a single clock cycle at a very high speed.

If the value of match bit (M) is logic '0', then it is bit value. Depending on the search line and bit line matching, the match line is made to be logic '1'. The signals from the Fredkin gate is sent to 3 × 3 Peres gate that executes the operation of the match-line. In Peres gate, input C is made as 0 so that output of the Peres gate be logical 'AND' operation between the earlier matched line in the row and the match line of the present TCAM cell.

Table.1. Functional table for RTCAM

Stored Data Bit	Search Data Bit	Match Bit Mb	Match-line State
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

So, if the earlier values of the matched line are low, then the match line for the entire row will be made low. If the match line in all the TCAM cells is high, then the match-line will become logic '1'. If at least any one of the match-line of the TCAM cell is low then the match-line of the whole row will be at low that resembles the operation of the classical TCAM cell.

In order to provide the WL signals for the functionality of TCAM cell to happen, we employ here SRAM. Instead of a conventional SRAM, a new design using reversible logic is proposed as shown in figure 6. It is evident from the figure 6 that quantum cost of the SRAM cell slightly increases but compromised for performance of the cell.

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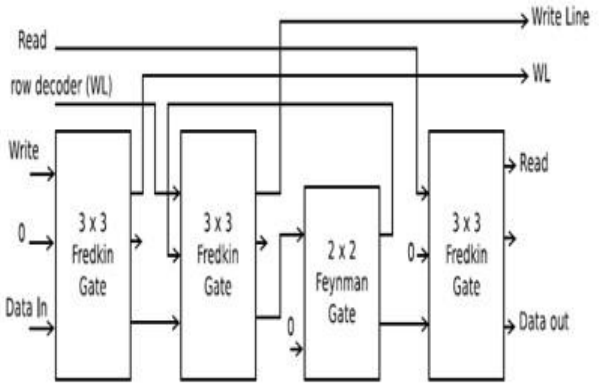

Fig.6. Basic SRAM Cell using Reversible Logic

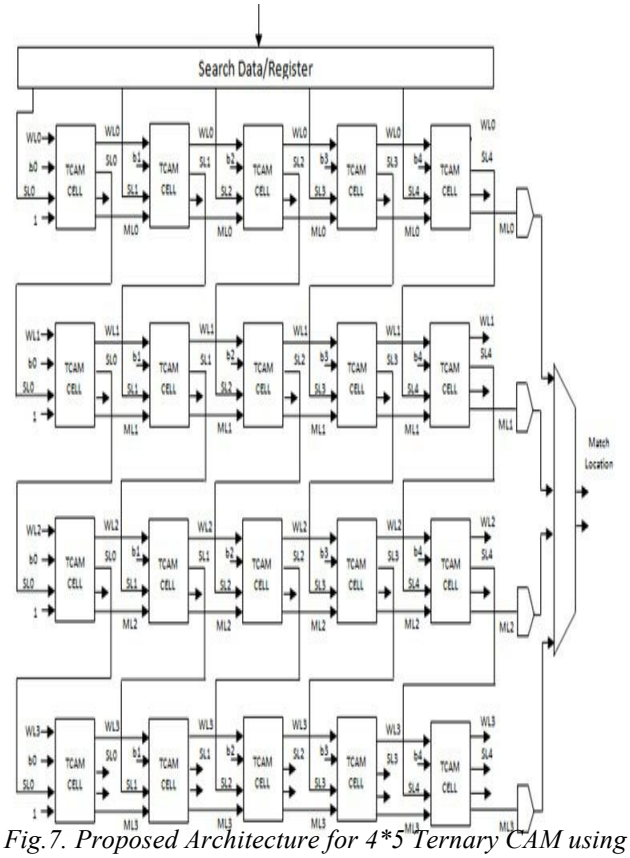

*Fig.7. Proposed Architecture for 4*5 Ternary CAM using Reversible Logic*

Figure.7 shows the proposed 4 × 5 reversible TCAM array. The data is copied into corresponding TCAM cells using with classical SRAM operation. After storing the data in the TCAM cell(s), match bit will be set to either logic '0' or logic '1' depending on whether the stored value is bit or don't care. Search data is sent to the respective TCAM cell from search data registers. Let us assume the data available in the 1st row of the TCAM array is 0011X and the data in the search line is 00101. Search Line1 data that is 1 is ex ored with data value that is 1. So the output of the ex-or operation is 0. When the data matched with the output of the ex-or operation is 0, it is then complemented to get the output 1. This features the operation of a classical binary CAM cell. The data saved in the TCAM is either logic '0'/logic '1' or 'X' depending on the value of the match bit

V.IMPLEMENTATION

This section is about the design metrics and synthesis performed in Xilinx 1SE 14.4.

Table.2: Design Metrics for Reversible Ternary CAM

Reversible Logic	Garbage Output	Constant Input	Gate Count	Quantum Cost
SRAM	2	1	2	9
SRAM(R/W)	3	3	4	16
TCAM	6	4	6	17

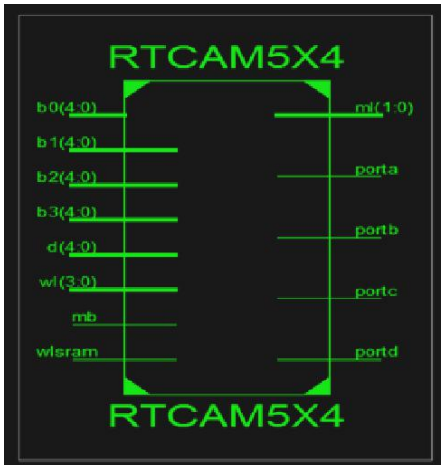

Fig.8. Entity for Reversible Ternary CAM

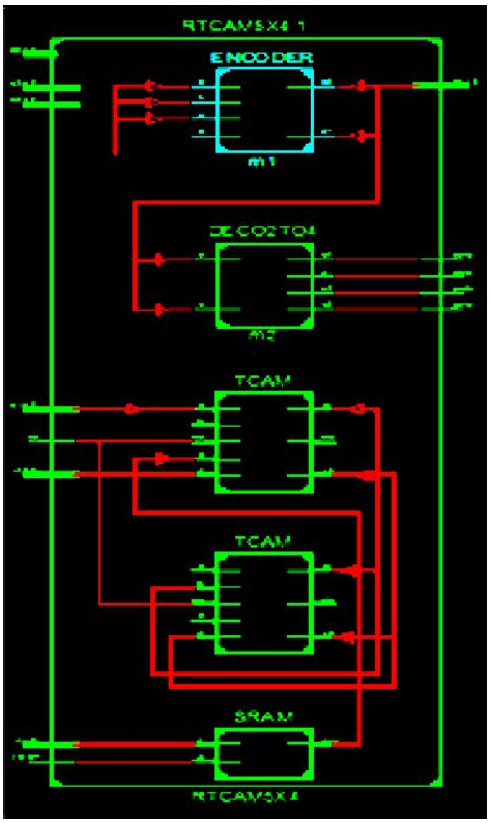

Fig.8. RTL Schematic for Reversible Ternary CAM Using Reversible SRAM and Combinational Logic

RTCAMSX4 Project Status (11/02/2016 - 04:21:31)			
Project File:	RLGS_TCAM.xise	Parser Errors:	No Errors
Module Name:	RTCAMSX4	Implementation State:	Synthesized
Target Device:	xc3s500e-4fg320	• Errors:	No Errors
Product Version:	ISE 14.4	• Warnings:	118 Warnings (5 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	29	4656	0%
Number of 4 input LUTs	50	9312	0%
Number of bonded IOBs	31	232	13%

Fig.9. Device Utilization Summary for 4X5 Reversible Ternary CAM

VI. SIMULATION RESULTS

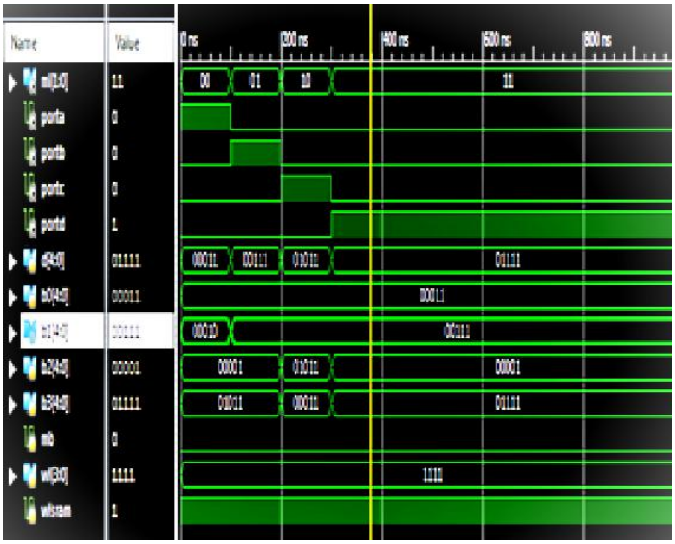

Fig.10. Device Utilization Summary for 4X5 Reversible Ternary CAM

VII. CONCLUSION AND FUTURE SCOPE

This paper proposed unique design of 4x5 TCAM array using reversible logic.

TCAM compares input data with stored data (logic '0', logic '1', don't care) in parallel and sends the matched data through outputs. In reversible SRAM design, 3 × 3 Fredkin gate and the 2 × 2 Feynman gate is used to create an SRAM cell. Each and every SRAM cell will have a word line (WL) to make the SRAM cell to operate in either 'read/write' or 'hold state'. A 3×3 Fredkin gate and Peres gate are used to perform the search line and match line operation. The design is functionally verified and simulated by using Xilinx ISE ISIM simulator. The practical realization of reversible TCAM will definitely minimizes the power consumption of the network switches. In future, optimized design of the reversible TCAMs may be used in place of conventional RAM in mobiles and computers to increase the speed of operation of the device without compromising for cost and area.

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