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IMPLEMENTATION OF A RECONFIGURABLE DELTA-SIGMA MODULATOR USING PSOC

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Abstract— **In this paper, a strategy for outlining reconfigurable discrete-time Delta-Sigma modulator topologies is proposed. Topologies are created from an arrangement of every single conceivable topology communicated by a bland topology, and enhanced for limiting the unpredictability of the topologies, amplifying the topology strength concerning circuit non-idealities, and limiting aggregate power consumption. The paper shows a contextual analysis for outlining topologies for a three-mode reconfigurable Delta-Sigma modulator. The paper likewise offers a reconfigurable topology implementation on a Programmable System-on-Chip gadget.**

Keywords— **Modulation, Capacitors, Signal to noise ratio, Sigma-delta modulation**.

I. INTRODUCTION

The improvement of reconfigurable innovation and System-On-Chip innovation are new concepts and philosophies, for example, Programmable System-On-Chip (PSOC), system level plan, and equipment/programming co-outline have been brought to microelectronic system outline. To stay aware of the quick changes in innovation, numerous colleges around the globe have started new courses or refreshed their current educational module for microelectronic system plan education. A large portion of these courses as a rule give careful consideration to computerized system plan than to simple or blended flag system outline. As the characteristic world is simple, it takes after those great deals of systems are simple or blended flag systems. Cases incorporate vehicle control and estimation systems, for example, car control guiding; therapeutic treatment gear, for example, electrocardiography, modern temperature or stream estimation and control system, Computerized Numerical Control controllers; and consumer electronic gadgets, for example, aeration and cooling systems. With its quick economic advancement, understudies and specialists must be gifted in the field of computerized electronics, as well as in that of simple or blended flag electronic circuit and system investigation and plan.

II. Implementation of a second-order reconfigurable topology on PSoC

PSoC is a true programmable embedded SoC integrating configurable analog and digital peripheral functions, memory and a microcontroller on a single chip. With an extremely flexible visual embedded design methodology that includes preconfigured, user-defined peripherals and hierarchical schematic entry.

We utilized the proposed plan philosophy to produce improved reconfigurable Delta-Sigma modulator topologies that fulfill various specifications, and have diminished system many-sided quality. The modulator works in three modes that correspond to UMTS, CDMA2000, and GSM communication guidelines. The DR necessity for UMTS, CDMA2000, and GSM are 11.5-piece, 13-bit, and 15-bit with the data transfer capacity of 1.92MHz, 615kHz, and 190kHz, individually [1].

The PSoC family consists of numerous blended flag clusters with on-chip controller devices. Simple PSoC square cluster consists of four simple sections, every one of which consists of three simple squares: one continuous-time (CT) square and two switched capacitor (SC) squares. The simple SC squares bolster Delta-Sigma, progressive approximation, and incremental ADC conversion, capacitor DACs, and SC channels. They have three input exhibits (ACAP, BCAP, and CCAP) and one criticism cluster (FCAP) of paired weighted exchanged capacitors, permitting client programmability of the capacitor weights. This gives summing ability of two scaled information sources and a non-exchanged capacitor input. ACAP, BCAP, and CCAP extend from 1C to 32C, and FCAP has estimation of 16C or 32C, where C is the unit capacitance of the capacitor cluster [6]. A second-order Delta-Sigma modulator can be actualized by utilizing two SC obstructs as the integrators. We outlined a double mode second-arrange topology. The objective peaks SNR for the two modes are 10 bits (60dB) and 8 bits (48dB), individually. The two modes have five and six flag ways with OSR of 64 and 40, individually. NTF composes for the two modes are Butterworth sort, and Inverse Chebyshev writes, respectively. At the point when the modulator is changed

starting with one mode then onto the next mode, four flag ways should be reconfigured: flag way coefficients a1,a2,b1 should be adjusted, and one more flag way t2,1 should be exchanged on for the second mode, as appeared in Fig. 1(a). The implementation of the topology on PSoC is appeared in Fig. 1(b). The coefficients (a1,a2,b1) of the flag way can be adjusted by changing the capacitor clusters (ACAP and FCAP). The additional flag way t2,1, when the modulator is reconfigured, is executed by utilizing one more input exhibit (BCAP) for the principal SC square. The estimations of the capacitor exhibits are appeared in Table-I. Fig. 2 demonstrates the simulation comes about. It demonstrates that the pinnacle SNR of the two modes equivalents to 71dB and 60dB for the perfect modulator, separately. On the off chance those circuits non-idealities are considered, the pinnacle SNR drops to 60dB and 54dB, separately, which can at present meet the outline specifications. Fig. 3 demonstrates the yield range from the estimation. The input is 2.1V peak to peak sinusoid wave with recurrence of 45kHz. For mode 1, the clamor floor level is about −55dB, and the SNR is around 60dB. For mode 2, the clamor floor level is about −47dB, and the SNR is around 53dB. Likewise, the indent of the Inverse Chebyshev NTF for the second mode is obviously appeared in Fig. 3(b).

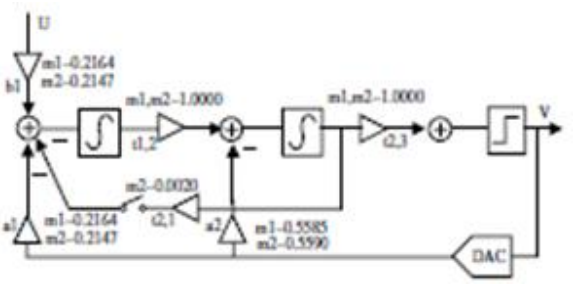

Fig. 1(a): Dual mode second order modulator topology

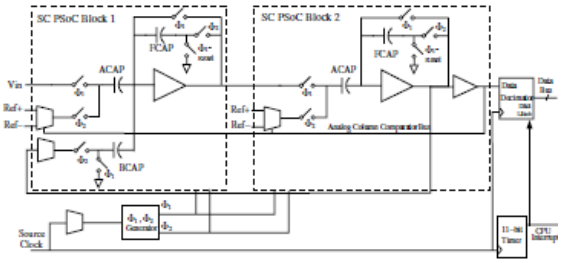

Fig. 1(b): Dual mode second order modulator PSoC implementation

TABLE I
Values for the capacitor array

Mode	SC Block 1			SC Block 2		
	ACAP	BCAP	FCAP	ACAP	BCAP	FCAP
1	4C	-	16C	8C	-	16C
2	8C	1C	32C	16C	-	32C

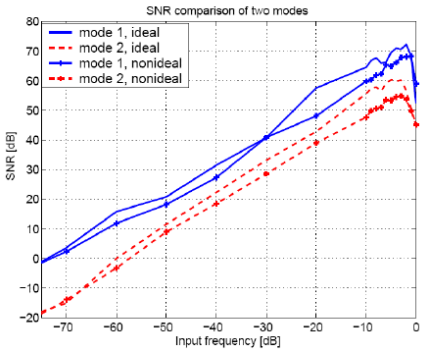

Fig. 2: SNR Comparison of Dual mode second order modulator

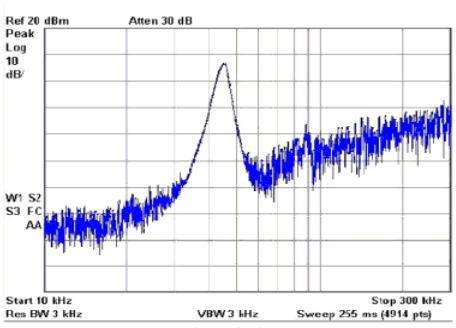

Fig. 3(a): Measurement result of mode1

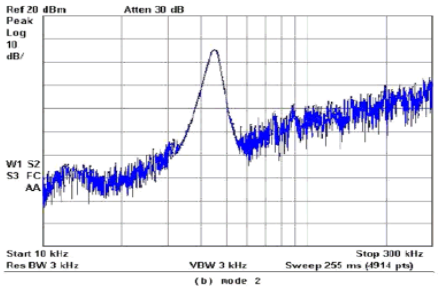

Fig. 3(b): Measurement result of mode2.

III. CONCLUSION

This paper displays a systematic procedure for outline of upgraded topologies for reconfigurable single-loop switched capacitor Delta-Sigma modulators. The approach streamlines the topologies for least many-sided quality, greatest power to execution degradation because of circuit non-idealities, and least power consumption. A contextual analysis on planning a three-mode reconfigurable Delta-Sigma modulator demonstrates that the intricacy and power sparing of the created reconfigurable modulators is around 40% and 24.2% of that of three single mode modulators got with Delta-Sigma tool kit. Generally essentially, the created reconfigurable topologies are more vigorous to integrator spillage and pick up blunder, circuit clamor, and nonlinearity than the topologies from Delta-Sigma tool stash. The dual mode reconfigurable topology is

additionally actualized on a PSoC gadget. Estimation comes about demonstrate that the modulator can meet the plan specifications.

REFERENCES

[1] R. H. M. Van Veldhoven, "A Triple-Mode Continuous-Time ΣΔ Modulator With Switched-Capacitor Feedback DAC for a GSMEDGE/ CDMA2000/UMTS Receiver", IEEE Journal of Solid-State Circuits,Vol. 38, No. 12, pp. 2069–2076, Dec. 2003

[2] F. Medeiro, A. Verdu, A. Vazquez, "Top-down Design of High Performance Delta-Sigma Modulators", Kluwer,1999.

[3] K. Francken, G. Gielen, "A High-level Simulation and Synthesis Environment for Delta-Sigma Modulators", IEEE Transactions on Computer Aided Design of ntegrated Circuits and Systems, Vol. 22, No. 8, 2003, pp. 1049-1061.

[4] O. Bajdechi, G. Gielen, J. Huijsing, "SystematicDesign Exploration of Delta-Sigma ADCs", IEEE Transactions on Circuits and Systems I, Vol. 51, No. 1, Jan 2004, pp. 86-95.

[5] H. Tang, H. Zhang, A. Doboli, "Refinement based Synthesis of Continuous-Time Analog Filters Through Successive Domain Pruning, Plateau Search and Adaptive Sampling", IEEE Transactions on CAD of Integrated Circuits and Systems, Vol. 25, No. 8, pp.1421-1440, August 2006.

[6] Technical Reference Manual, PSoC TRM, Version 2.00, Cypress Semiconductor Corporation.

[7] https://www.cypress.com/

[8] R. Veldhoven, "A Triple-Mode Continuous-Time ΔΣModulator With Switched-Capacitor Feedback DAC for a GSM/EDGE/CDMA2000/UMTS Receiver", JSS, Dec 2003.

[9] Hugo De Man, "System-on-Chip Design: Impact on Education and Research", IEEE Design & Test of Computers, July-Sept. 1999.

[10] A. Doboliand E. Currie "Embedded Mixed-Signal Systems: A Designer's Perspective", due to be published in 2007.