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Low Power Low Voltage 10-Bit Monotonic SAR ADC for Industrial Application

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***Abstract*— Analog to digital converters that operate at a low voltage and consuming low power is needed for various applications. This paper present a comparison of conventional SAR and a monotonic SAR. A Low Power Low voltage 10-bit Successive Approximation Register (SAR) Analog to Digital Converter (ADC), that uses a monotonic way of switching procedure is designed. It saves 50% of capacitance area and 71% of dynamic power. A Dynamic latch comparator is designed with minimum offset and power. In order to achieve high linearity transmission gate is used as switch. The design is implemented in 55LPE standard CMOS technology with power supply of 1.8V, the power consumption of 0.834mW. The proposed ADC achieved SFDR of 63.44dB, SNDR 52.07dB with area of 790 X 890 µm2.**

***Index Terms*—ADC, SAR, Dynamic Power, CMOS Technology .**

I. INTRODUCTION

In nature all the signals that are available around us are analog in nature. These signals are continuous in both time and amplitude. But for the sake of convenience in processing and the ease of implementation and cost factor most of the processing or computations are preferred in digital domain [2]. The digital signals are those which are discrete in time and in amplitude. Hence there has to be an interface that converts the input analog signal to digital. Once the analog signal is converted to digital it is processed. Now the processed digital data has to be converted back to analog signal so that the end user can perceive it. These interface systems that are used for the conversion of analog signal to digital and digital signal to analog are known as the data converters.

Analog signal to digital signal conversion is done by analog to digital converter [1-5] (ADC) and digital signal to analog signal conversion is done by digital to analog converter [1-5] (DAC) .Here we will discuss about ADC. For the conversion of analog signal to digital signal it is important that the conversion is performed with minimum loss of information. The conversion is performed in two steps. First the continuous analog signal is sampled to obtain a signal that is continuous in amplitude but discrete in time [1] .This step is known as sampling. Then the sampled values are mapped to suitable levels in order to obtain discrete amplitude. This step is known as quantization. In analog conversion the accuracy of the digitized signal depends on two parameters which are the number of samples taken and the resolution or the number of quantization levels. A better ADC is formed with more number of samples and more number of quantization levels. The lower limit of the number of samples is determined by the Nyquist criteria which states that the sampling rate has to be atleast equal to twice the highest frequency component present in the signal. When the sampled value is quantized if we consider more number of bits then the analog value can be represented with more accuracy .This is known as the resolution of the converter. The sampling rate determines the speed at which the Analog input can be converted to its corresponding digital code. Hence resolution and speed are two important aspects which are used in the selection of architectures [3]. There are different architecture of ADC available, the selection of the architecture is dependent on the user requirement. The selection of architecture is mostly decided by the resolution, sampling rates and the application in which the converter is desired to operate.Mostly if an application demands an N-bit resolution it is better to design the system for a resolution higher than this as the achievable accuracy is always less than the one for which it is designed.

II. LITERATURE REVIEW

The available ADC are Sigma delta ADC, pipeline ADC, Flash ADC, SAR ADC [11]. Sigma delta ADC are used for higher resolutions in the range 12-24 bit. These are used in digital and audio band and the sampling rates are up to 22 KHz. Flash ADC are available with sampling rates up to 1.5Gsps and with resolution up to 8 bit. SAR ADC have resolution ranging from 8 bits to 18 bits and sampling rates from 50kHz to 50MHz. Pipeline ADC are available with sampling rates in range of Giga samples and with resolution in the range of 8bit to 16 bit. The selection of right architecture is depending on application.

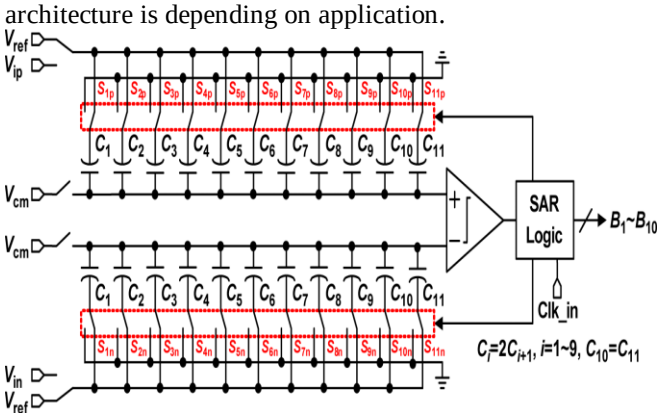

Figure 1.Conventional 10-Bit SAR ADC

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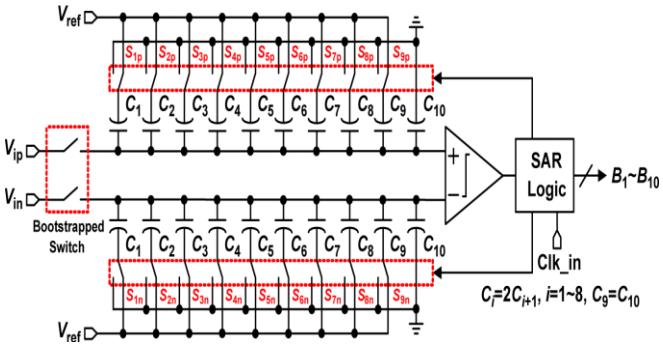

Figure 2. Monotonic 10-Bit SAR ADC

III. Proposed Architecture

SAR ADC is one with the lowest power dissipation. Also in the SAR ADC implementation operational amplifiers which is one of the greater power consumption blocks is not used. SAR ADC uses a simple algorithm known as binary search algorithm for arriving at the digital code corresponding to the analog input. Differential implementation of SAR ADC is done in order to reduce the supply noise and the common mode noise. To get an accuracy of 10-bit same architecture used in differential mode. It consist of comparator, SAR logic, Cap-Dac [4] network, and switch. In Fig 1 the Cap-Dac is work as a sample and hold circuit, it that binary weighted capacitance provide better linearity and CMRR [9] (Common mode rejection ratio).

Sample and Hold basically used separately in conventional ADC but in proposed architecture Capacitor Network will act as Sample and Hold both. Which result in reduce one block from the system design, How its work is totally depend on SAR logic and input switch the combination of both will act as Sample & Hold circuit. DAC is the circuit that convert digital input to analog values. In case of successive approximation ADC binary weighted capacitive DACs are used, there is no requirement of an additional sample and hold circuit when using a capacitive DAC as the DAC itself performs this operation. The input signals are analog in nature. Thus a sample and hold circuit is required to hold the input voltage at a value so that its corresponding digital code can be computed. Sample and hold circuit consist of a switch and a capacitor. It has two phase of operation which are the sample and hold phase. In the sample phase the switch is closed and the output capacitor C is charged to the input voltage that is it tracks the input voltage. In the hold phase the switch is closed and the sampled value is hold and it provides a constant voltage at the output. The output of this sample and hold circuit is given as input to the comparator. The sample and hold circuit effects the dynamic performance of the ADC like SNDR [9-11].

Sampled analog value. This is followed by up conversion or down conversion based on the comparator output. If the sampled input is greater than the DAC output value then an up conversion occurs else a down conversion occurs. In up conversion the MSB bit is retained and the MSB -1 bit is set as 1. In the down conversion the MSB bit is set as 0 and the MSB -1 bit is set as 1. Then the process of comparison of the equivalent analog value with the sampled input is done and the cycle continues. An n bit ADC n such cycles are performed to arrive at an n bit digital code for the sampled input. Once the input code is converted to the corresponding digital code an End of Conversion (EOC) signal is set to mark the completion of the analog value to digital conversion. SAR ADC involves two clocks which are the global clock and the bit cycling clock. The global clock has two phases of operation which are the sample and hold phase. In the sample phase the analog input value is sampled by the sample and hold. During the hold phase the conversion process happens. In the hold phase the number of cycles depends on the number of bit resolution of the SAR ADC. An n bit ADC takes n clock cycles in the hold phase to complete the conversion.

The SAR logic Fig. 3 operates on the basis of the output from the comparator. SAR logic is based on binary search algorithm. It is like the entire range is first divided into two parts and it is checked if the input lies in any of these range. Then the range in which the input falls is further divided into two parts and it is checked if the input lies in this range. The process of doing this is for an n bit SAR ADC. First the nth bit i.e. the MSB bit is set as logic 1 in the SAR logic register. Then the equivalent analog value for this is generated using a DAC. This analog value generated is compared with the input

In proposed architecture Fig 2 number of capacitance require is half of the conventional one in the conventional switching procedure switching is optimum if all the conversions are up conversions. But if the comparator output is 1 then the bit that is set in the cycle has to be reset to 0 and the next bit position has to be set to 1. Hence there is extra switching that is happening. The switching consumes a lot of power [6]. Hence the switching has to be minimized and hence we go for the method known as monotonic capacitor switching procedure. In this the amount of switching is reduced by 71 % and the total capacitance is reduced by 50%.

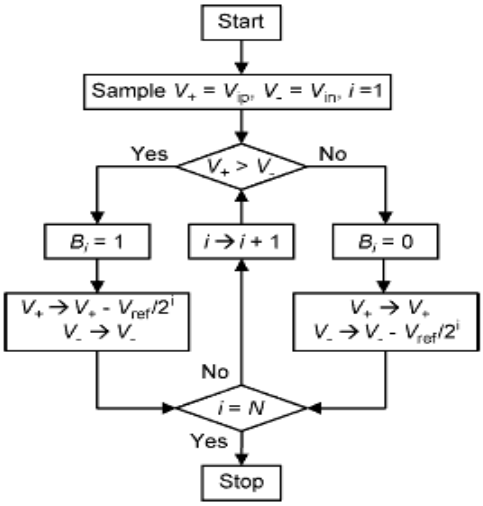

Figure 3. SAR Logic

In the sampling phase the top plates of the capacitor array will be connected to Vin and the bottom plates will be connected to V_{ref}[7]. Consider a 3 bit operation. In the sampling phase Vinp and Vinn are connected to the top plate of the capacitor and the bottom plates are connected to Vref. The voltage across the capacitor array connected to the positive terminal of the comparator is Vinp – Vref and at the negative terminal is Vinn – Vref. The charge at the top

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capacitor array is (Vinp – Vref) 4C and the charge at the bottom plate of the capacitor is (Vinn – Vref) 4C. The comparator directly performs the comparison now without any switching.

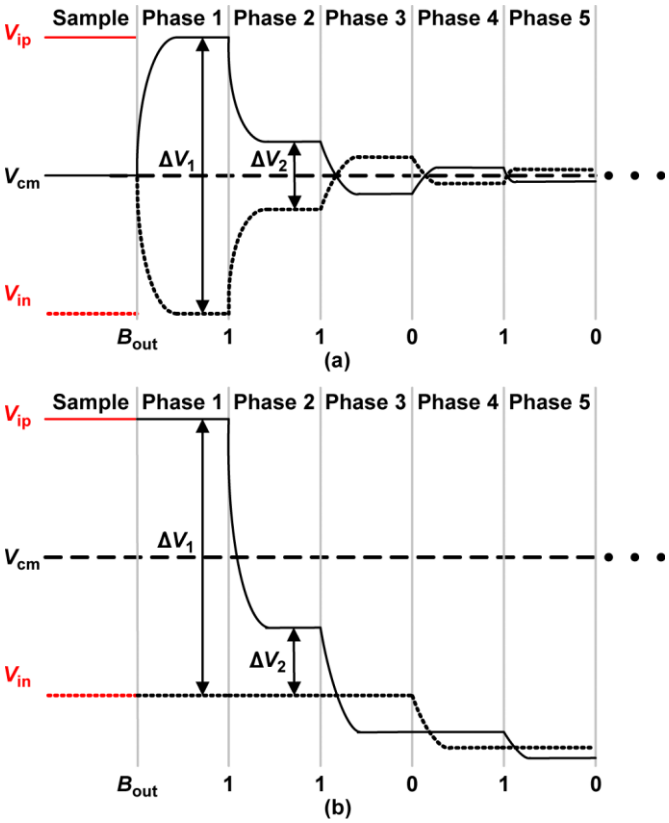

Figure 4 Output waveform of (a). Conventional SAR & (b). Monotonic SAR ADC

Vinp – Vref > Vinn – Vref
i.e Vinp > Vref
If Vinp > Vref then the comparator output is set as 1. Then the MSB capacitor in the top capacitor array is reset and connected to ground. The MSB capacitor at the bottom array is maintained at Vref.
According to charge conservation the charge across the capacitor is conserved. Hence
(Vxp – Vref) 2C + Vxp * 2C = 4C (Vinp – Vref)
Hence Vxp = Vinp – Vref/2
(Vxn – Vref) 4C = 4C (Vinn – Vref)
Hence Vxn = Vinn (1)

In the next cycle Vxp is compared with Vxn
Vxp > Vxn i.e Vinp – Vref/2 > Vinn
The comparison in second cycle is Vinp – Vinn > Vref/2
The node voltage at the positive terminal of the comparator is reduced by Vref /2 and the node voltage at the negative terminal is maintained at the initial value. Comparator output is now 0. In this cycle if Vinp - Vinn < Vref /2 then the second capacitor at top capacitor array is retained at Vref and second capacitor at the bottom capacitor array is reset and connected to ground.
According to charge conservation
Vxp * 2C + (Vxp – Vref) 2C = 4C (Vinp – Vref)
Vxp = Vinp – Vref/2 (2)
(Vxn - Vref) 3C + Vxn * C = 4C (Vinn – Vref)
Vxn = Vinn – Vref/4 (3)

The comparator the performs the comparison
Vinp – Vref/2 > Vinn - Vref/4
Vinp – Vinn > (3/4)*Vref
Thus the voltage at the comparator positive terminal is maintained in Fig.4 and the voltage at the comparator negative terminal is reduced by $V_{ref}/4$.

IV. Conclusion

A SAR ADC uses Monotonic way of switching action. This implementation has enabled the reduction in area by 50% and power by 71%. A dynamic latched is used by which a reduction in power and MOS area is achieved. Here transmission gate is used as switch to improve the performance of overall system at high frequency as well as low frequency. The SAR logic for monotonic SAR ADC designed is written in Verilog HDL so that it can be easily interfaced with the Analog block.

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