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A Review on various types of design of Multiplier

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***Abstract*—In this paper, a design of 32x32 bit using 4 bit bit-sliced integer multiplier is proposed. Rapid Single Flux Quantum (RSFQ) technology is implemented for its high speed and low power consumption. As in every digital circuit addition and multiplication are two most essential mathematical operations. With the increase in circuit complexity and hardware cost bit slice approach is used. In this paper, we will discuss a various methods of designing the multiplier.**

Keywords*—Rapid Single Flux Quantum (RSFQ), Quantum Technology

I. INTRODUCTION

Multiplication is one among the fundamental and demanding operations within the computations. Efficient implementation of multipliers is needed in several applications. The multiplier plays an important role in much DSP application because it dominates the chip power consumption and speed of the operation. If proper optimized multiplier is not used in any digital circuit it consumes more power and will produce the lag. There are various types of design of multiplier with different algorithm and structures. To get a better performance parameter different multipliers are designed with different performance parameter. In recent years, superconducting RSFQ method is one of the most trending integrated circuit technologies which is especially known for its high speed and low power consumption.

Bit serial architecture has lower complexity as it takes longer calculation time to process 32-bit data whereas, parallel architecture requires larger hardware cost. So here in this paper we have used the bit slice architecture where data are divided into several slices of several bits each. As here the data is divided in various parts it will process faster as compared to that in bit serial architecture where data is moving serially. Bit slice architecture is preferred over bit serial architecture so that can give the better solution to RSFQ multipliers. So bit slice methodology is used while designing the multiplier.

RSFQ stands for Rapid single flux quantum. It is a digital signal logic used to store data in the form of magnetic flux quanta and later convert them into Single Flux Quantum (SFQ) voltage pulses .In static SFQ circuits, the information is passed in the form of dc flux . These devices are of a high fundamental interest because of their capability to implement the reversible processing of digital information. RSFQ circuitry is essentially self clocking, making asynchronous designs much more practical. These are used in superconductors and require extremely cooling conditions for operating. It is a possible choice for semiconductor devices which are working on low power and high speed digital mixed signal applications. The major area of RSFQ logic is digital signal processing (DSP) where it works for applications like digital multipliers, accumulators and digital filters. There are various types of design of multipliers used are array multiplier, booths multiplier, Wallace multipliers, Dadda's multiplier

II. ARRAY MULTIPLIERS

Array Multiplier is usually based on its regular structure which uses add and shift algorithm. Although it has pipelining structure which can be easily scalable. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added.[2]

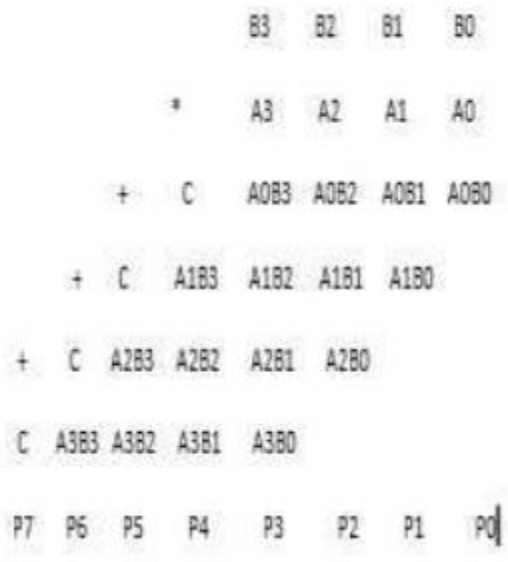

Fig: Array Multiplier structure[2]

III. BOOTHS MULTIPLIER

A new algorithm was invented by Booth Donald Booth (1950) of multiplying two signed (or unsigned) numbers which reduces the partial product generation of the multiplier. Encoding of multiplication and partial product generation in done in Booths multiplier. For improving the performance of the multiplier the partial product can be decreased. The selector address is used to decrease and reconstruct the partial product in the construction of modified Booths multiplier. To enhance the performance of the multiplier system pipelining approach is introduced. The multiplicand (A) bit and multiplier (B) bit is provided to the partial product generator (PPG) for generating the number of partial products.

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Modified Booth multiplier exhibits pipeline approaches which contain three major modules, the T/2partial products are generated by the modified Booth encoder multiplier and modified Booth decoder multiplier. The second one is the Wallace algorithm and the third is, the CLA adder is used for final addition. Excessive power consumption of the booths multiplier is the major drawback of the Booths multiplier.

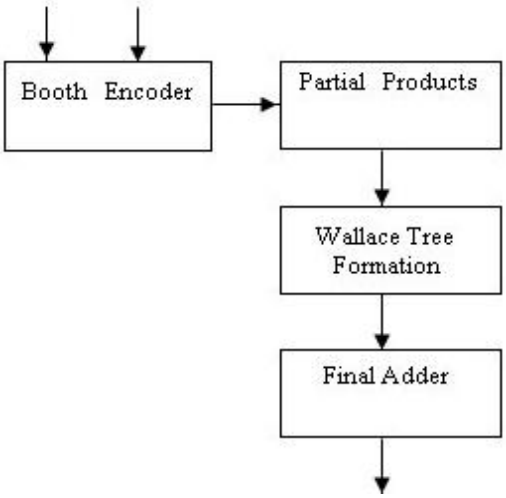

Fig: Booths Multiplier

IV. WALLACE MULTIPLIER

The Wallace multiplier is the fastest process for multiplication of two digit number. The steps to be followed for the multiplication of two numbers. At the initial steps bit products are generated and in next steps reduce the product matrix into the row matrix. Whereas Bit products are equal to sum of two rows. In the last step the fast adder are used for summing of two resulting rows to generate final product.

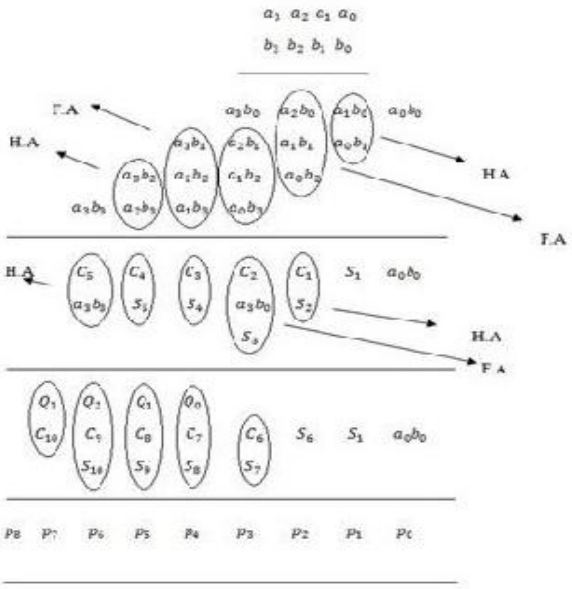

Fig: Wallace Multiplier Structure

V .LITERATURE SURVEY

Guang-Ming Tang, Pei-Yao Qu, Xiao-Chun Ye, Dong-Rui Fan, and Ning-Hui Sun have presented a 32-bit 4x4 bit slice RSFQ matrix multiplier. The multiplier performs operation on unsigned integer matrix multiplication. The bit serial processing requires greater latency as compared to parallel processing whereas parallel processing leads to higher hardware cost. So, bit slice processing achieves higher speed than bit serial processing and less hardware cost than parallel processing. The proposed methodology states that each of the 32 bit element in A and B is divided into four slices of each eight bit. In this paper they have used concurrent flow clocking to design fully pipelined synchronous RSFQ logic circuits of the matrix multiplication. They have used type of parallel prefix adder called Sklansky adder to implement it. This block consist of six pipelined stages. The delay is present in the feedback loop is for the carry signal to the succeeding slice. They have designed the logic circuit 2/-4/-8/-16- bit slice and parallel matrix multipliers without considering the delay of Josephson transmission line(JTLS), passive transmission line and splitters. They have found that performance of the proposed matrix multiplier is better than CMOS matrix multiplier.[1]

N.Fahmina Afreen, M.Mahaboob, S.Mohan Das have presented that performance of multiplier depends on adder. So there is immense need of using an efficient adder for multiplication. To enhance the performance of DSP system definitely an efficient adder is utilized. This paper presents lower area, energy efficient 32 bit Array Multiplier. By minimizing the area and power the performance of the DSP system can be enhanced. The proposed system overcomes the CSLA and BEC based CSLA, optimized CSLA has been introduced. The simulation waveform of the proposed method was observed on Xpower model. The power consumed by three different design of CSLA and Multiplier were carried by Xpower model. The proposed adder have been implemented by eliminating the repeated logic function from BEC based Optimized CSLA. Efficient multiplier have been designed and designed multiplier were modeled with Verilog. It is observed from the verified results that as compared to conventional CSLA based multiplier, the Optimized CSLA multiplier involves less area, LUTs reduced by 7.6%, less delay(reduced by 7.6%) and low power consumption(reduced by 41%). To improve the performance of the system convolution is utmost mathematical operation which required efficient addition and multiplication.[2]

Guang-Ming Tang, Kazuyoshi Takagi and Naofumi Takagi have presented a 4-bit bit slice multiplier for a 32 bit rapid single flux quantum (RSFQ) microprocessor. They proposed multiplier of each 32 bit multiplicand X and multiplier Y which is divided into eight slices of 4 bit each. Then eight pairs of operand slices are given input to LSB. It performs operation on 32x32-bit signed and unsigned integer multiplication. Then the output of 64 bit final product Z is in sixteen 4bit slices which are output one by one from LSB. In this paper for the proposed design of multiplier they have used the concurrent flow clocking technique. They have used a fully pipelined synchronous RSFQ logic in which each pipelined stage consist of RSFQ clocked logic gates. So as per proposed methodology of multiplier 4-bit bit sliced multiplier for 32 bit microprocessor is designed using RSFQ

logic design which consist of17,551 JJs. The simulation results where found correct at 62.5Ghz. ALCA-JST in Japan partly supported this work.[3]

Guang-Ming Tang, Kazuyoshi Takagi presented a design of 32x32 bit 4-bit bit sliced integer multiplier for rapid single flux quantum microprocessors. The multiplier carries out both signed and unsigned integer multiplication. It uses a concurrent flow clocking and target frequency of 50 GHz using AIST 1.0-um Nb/AlOx/Nb. As it uses a bit slice approach which simplifies circuit complexity and reduces the hardware cost. They proposed a design of 32x32 bit 4-bit bit slice integer multiplication. Previously the 11x11-bit-bit serial multiplier was designed as a component of floating point multiplier and 8x8-bit parallel unsigned integer RSFQ multiplier. But no bit slice RSFQ multiplier has been developed. The multiplier proposed in this paper based on synchronous concurrent flow clocking, so that slices are proposed in pipelining. They have observed that in 32 bit parallel processor the hardware cost of component circuits of a 32 bit parallel processor is to high for the current RSFQ technology. However they have preferred to use bit slice processing rather that parallel processing for 32 bit microprocessor. Design of 32x32 bit 4-bit slice multiplier is designed using the AIST ADP2 in which physical design consist of 56,885 JJs, and occupies an area of 12.00x6.65mm^2. The simulation results is observed at 50 GHz, and throughput of the multiplier is 3.25x10^6.[4]

Guang-Ming Tang have presented the design of 4-bit bit slice matrix multiplier for 32-bit rapid signal flux quantum (RSFQ) artificial intelligence processor. It mainly consists of 4 bit-bit slice multipliers and bit slice adders. The multipliers perform unsigned integer matrix operation which is implemented by control signals. The proposed matrix multiplier use concurrent flow clocking to design a fully pipelined synchronous RSFQ logic circuit. The pipeline stage consists of row of RSFQ clocked logic gates. For holding slice of A0-A3 register is implemented using eight D flip flops. They have also used bit-slice multiplier and bit slice Sklansky adder. In matrix multiplier there are in total 45 stages and only one I-stage feedback loop which is in a 4 bit-bit slice adder. The proposed matrix multiplier consist of 72,148JJs.[5]

Qingzheng LI, Guixuan LIANG, Amine BERMAK have presented the design of high speed signed and unsigned pipelined multiplier. A novel unified implementation of signed/unsigned multiplication is proposed using a simple sign-control unit together with a line of multiplexers. CMOS implementation of a 32-bit signed/unsigned multiplier. In this paper, first stage is utilized using modified booth encoding in order to reduce the partial product rows (PPRs) by half. To efficiently sum up PPRs using carry-save adders the second stage comprises of two-level Wallace-tree compression structure. The final two partial product rows are processed by a hybrid adder mixed with conditional carry adder (CCA) and conditional sum adder (CSA) based on the MLCSMA algorithm. By developing more efficient compression methods and combining several types of fast adders the multipliers can be optimized in terms of speed, power. The proposed multiplier calculated critical path is about 3.13ns.[6]

V.Vijayalakshmil, R.Seshadd, Dr.S.Ramakrishnan have presented 32 bit unsigned multiplier using CSLA and CLAA. In the comparison of the carry look ahead adder and carry select adder based 32-bit unsigned integer multiplier. The CLAA multiplier and CSLA multiplier uses the same delay for multiplication. The complexity of the CLAA multiplier is reduced to 31% by the CSLA based multiplier to complete the multiplication operation. Due to parallel generation of the carry bits carry look ahead adder produce carries faster by using the additional circuitry. This adders are slower and its carry propagation time is reduced results in the use of least energy. In CSLA adder computation of alternative results with single or multiple stage is done. In the CSLA multiplier time taken to calculate the sum is avoided which results to the increase in speed. The proposed multipliers are implemented using Altera Quartus II and timing diagrams are viewed through avan waves[7].

V. CONCLUSION

The power consumption of multipliers and the basic building block of more CMOS VLSI circuits depend on the switching activities of the adders. Hence the interests on various design techniques of such low power circuits have increased in the recent past. This review paper is focused on the different techniques used to implement multipliers and also give a power analysis of multipliers to identify the improved architectures for low power applications. It was also analyzed and studied that bit sliced multipliers used for RSFQ microprocessor applications are good with respect to speed and time delay. Bit sliced multipliers also optimizes the circuit complexity and reduces the hardware cost.

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